# Winter School: SERENA, Car2Tra, GRACE Technology and Integration Platforms for Future mm-wave Communication and Radar Applications

## *Silicon technology trends*

Franz Dielacher
January 2020

# OUTLINE

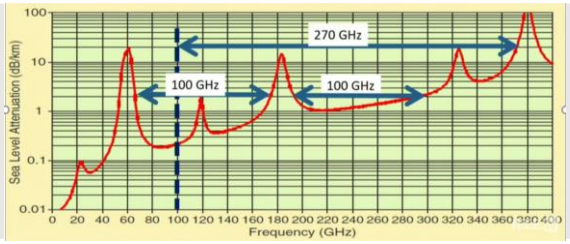
- Introduction
  - Market trends and RF requirements
- Technology Roadmap and Moore's Law
  - ITRS (IRDS)
  - CMOS / FinFET / FDSOI / SiGe-BiCMOS
  - SCALING
- SiGe-BiCMOS process flow
- Next generation transistor architectures (new technologies)
- Summary

# Future Trends and Technology under Investigation

Applications

Technology

**mmWave Comm.**




Where to find the spectrum for 1 Tb/s

**Automotive Radar**

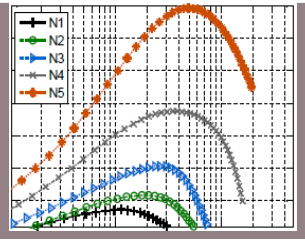
24GHz, 76-77GHz today
79GHz, 122 GHz in the future
In cabin monitoring, Road surface det.
Automated driving

**Security Medical Scanning**

A lot phenomena in solids, liquids and gases occur in the THz domain

- Industrial analysis
- Astrophysics, Atmospheric, Chemistry
- Biomedical, detect bacteries, …

**SiGe RF-CMOS III/V**




SiGe: $f_{max}$ = 400 GHz today, 600 GHz soon
RF-CMOS: FDSOI, FinFET, Nanowire - future
III/V: for THz and high output power

**Frequency**

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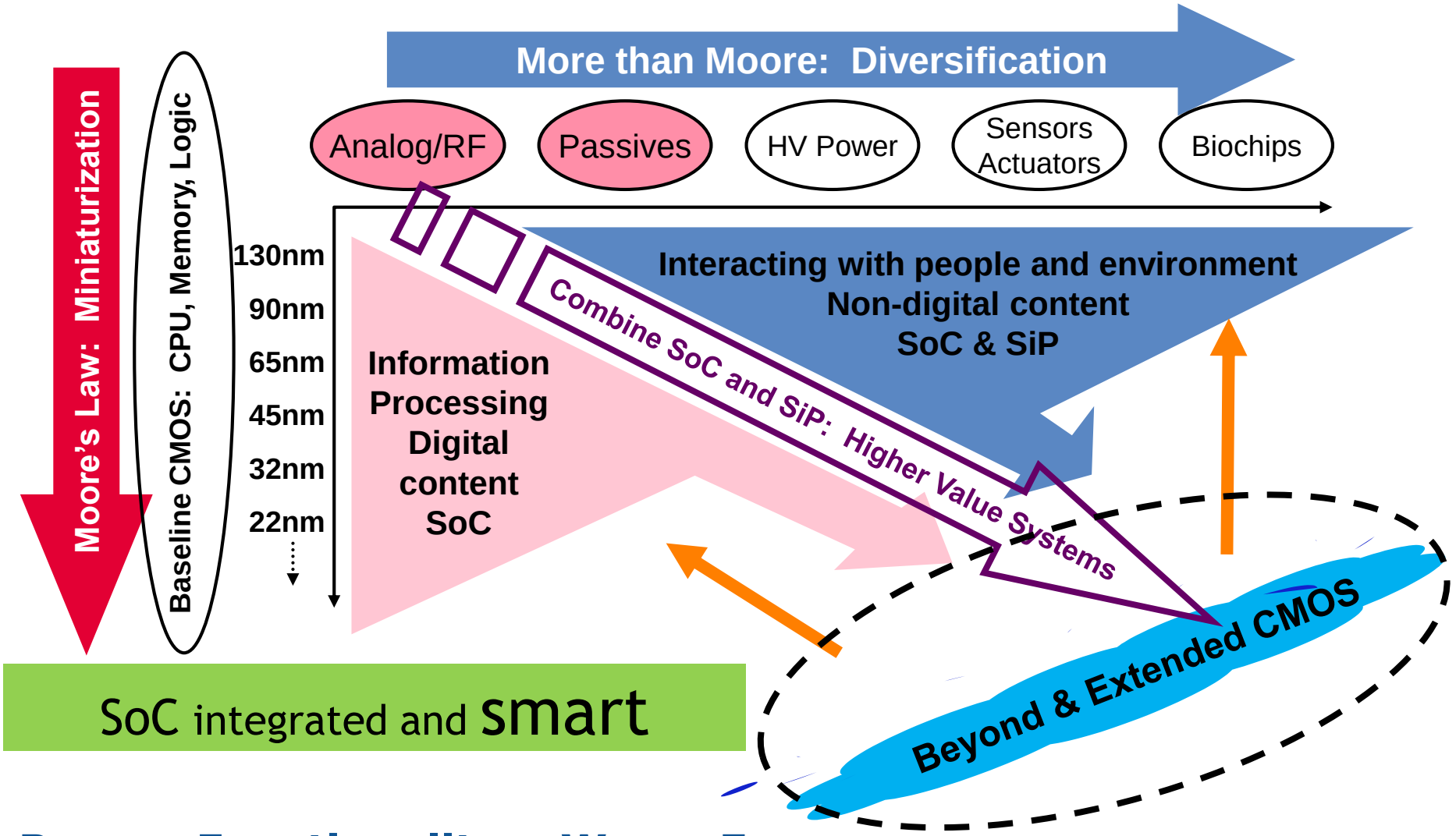
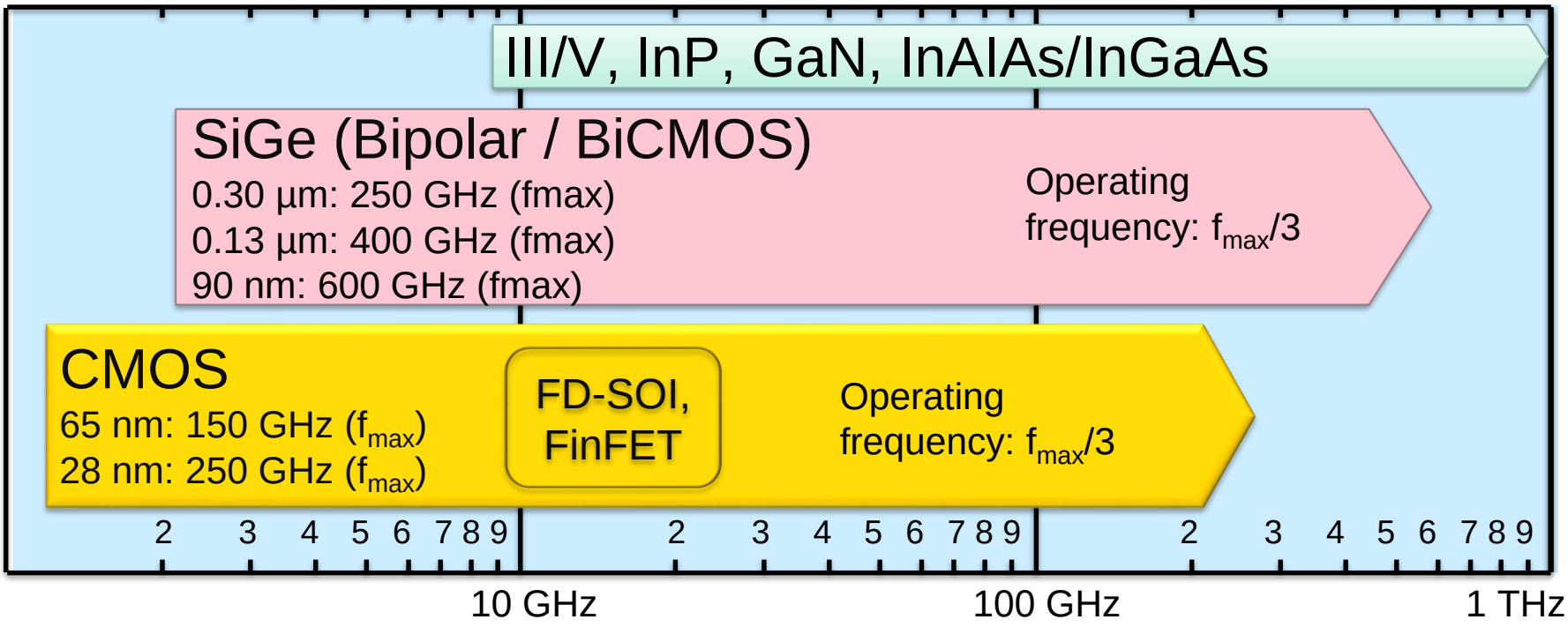
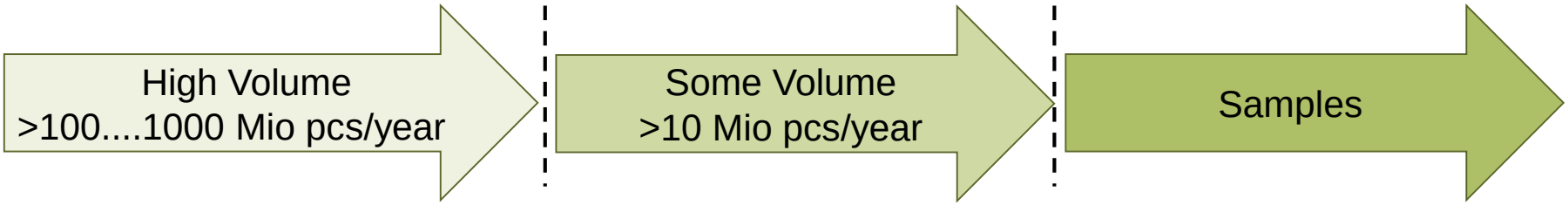
# Technology Roadmap and Moore's Law

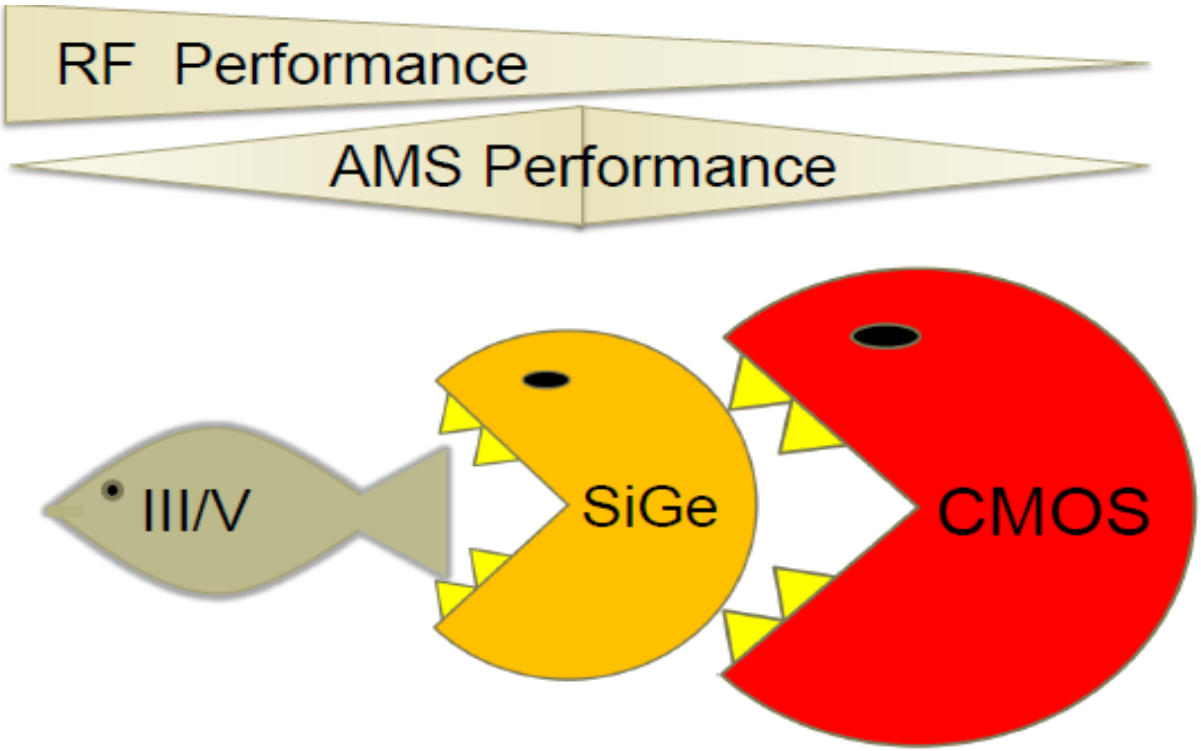


# Technology Choice – focus on RF



# Food Chain

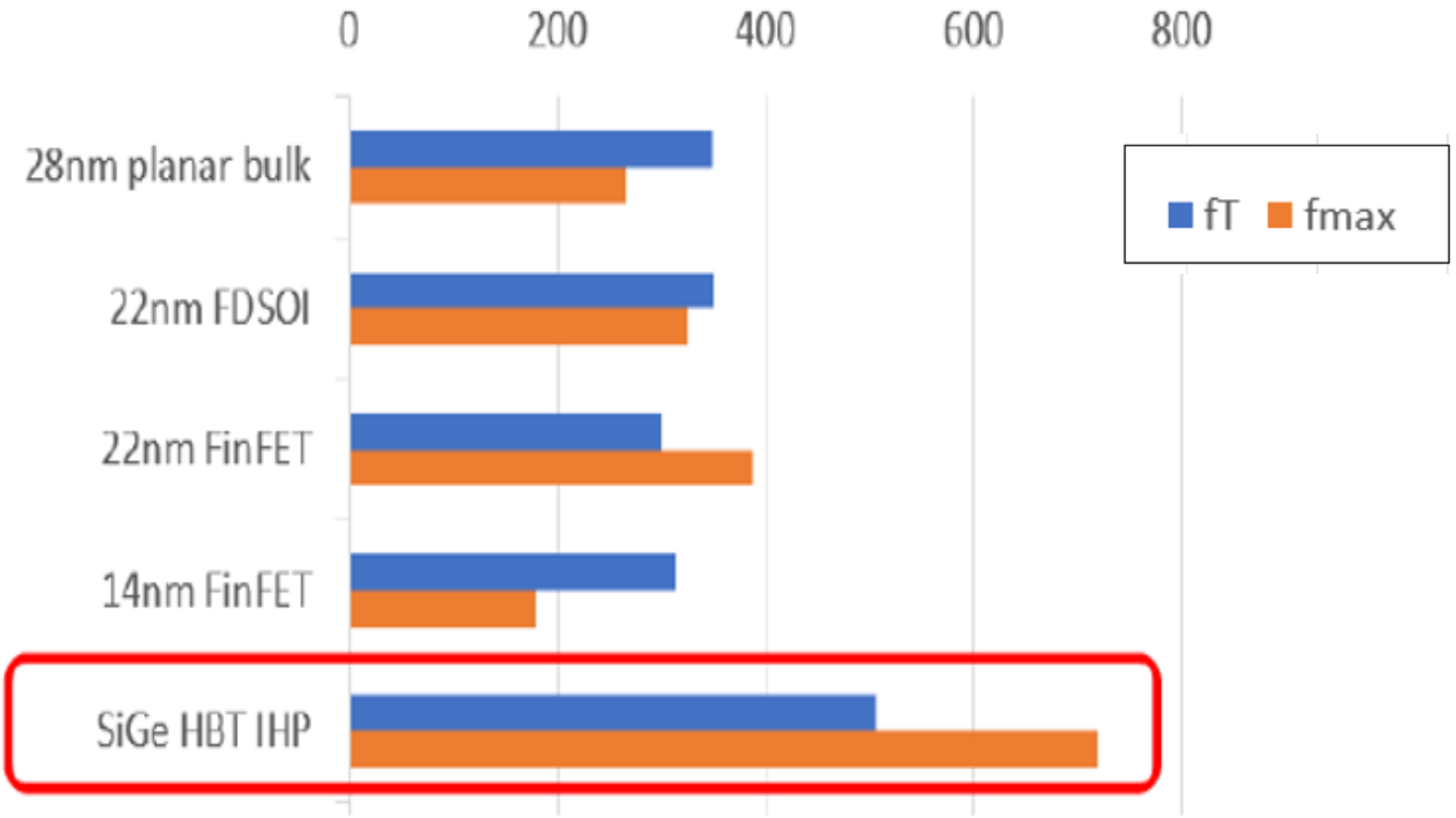



1st Law:
What can be done in Silicon, will be done in Silicon

2nd Law:
What can be done in CMOS, will be done in CMOS

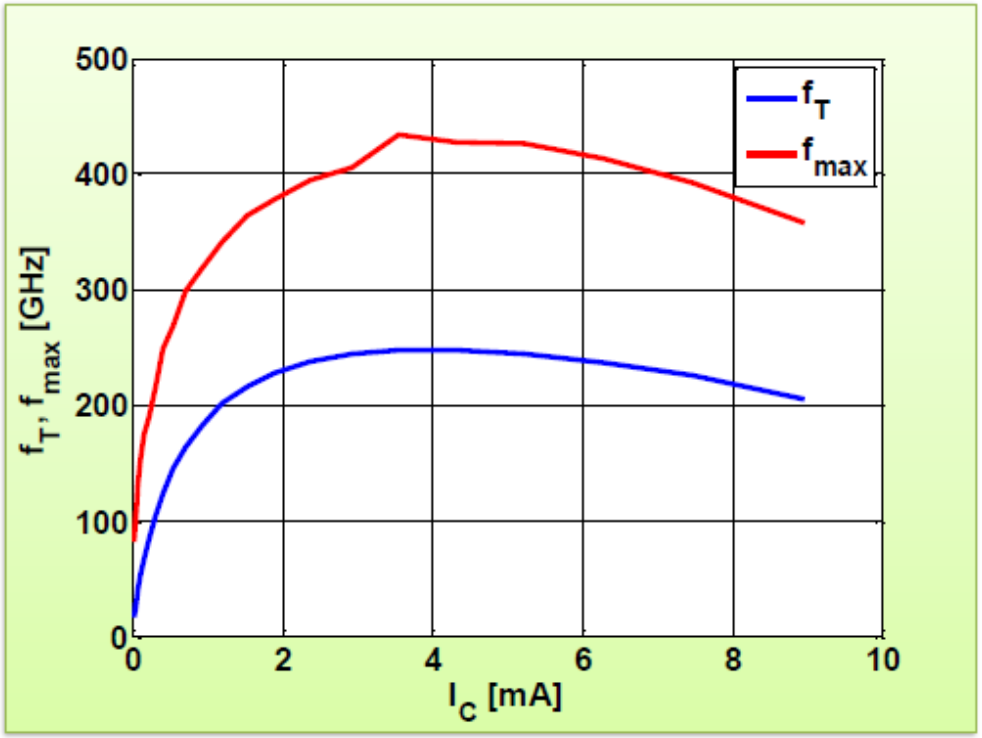
**…if there is a business case**

# State of the Art Silicon Technologies




CMOS speed is saturationg: $f_T/f_{MAX}$ limited to < 500 GHz

# Infineons status today
# SiGe BiCMOS for high speed and high VDD




**130nm SiGe-BiCMOS:**
**$f_{max}$ = 435 GHz**
**$f_T$ = 250 GHz**
**$J_C$ ~ 13 mA/µm²**
**AE = 0.2 x 2.8 µm²**
**Min. Gate Delay ~ 2.3 ps**
Substrate: p, 20 Ωcm, 8“
Base Layer: SiGe:C
**Metallization:**
**6 L Copper /1 L Top Al**

| $BV_{ceo}$ | $BV_{cbo}$ | $BV_{ebo}$ |
|---|---|---|
| 1,5V | 5,3V | 2V |

# CMOS/BiP/BiCMOS Technology Comparison

| | FinFET | FD-SOI | SiGe (BJT) |
|---|---|---|---|
| Gain | + | - | + |
| Series Resistance | - | + | + |
| Speed | - | + | + |
| Compatibility with CMOS | - | + | - |
| Towards 5nm | + | - | - |
| Supply Voltage | - | - | + |

SiGe-HBT: 4x better gm/IDS, Higher voltage (output power), …..

FD-SOI: Dynamical modulation of threshold voltage of devices, .....

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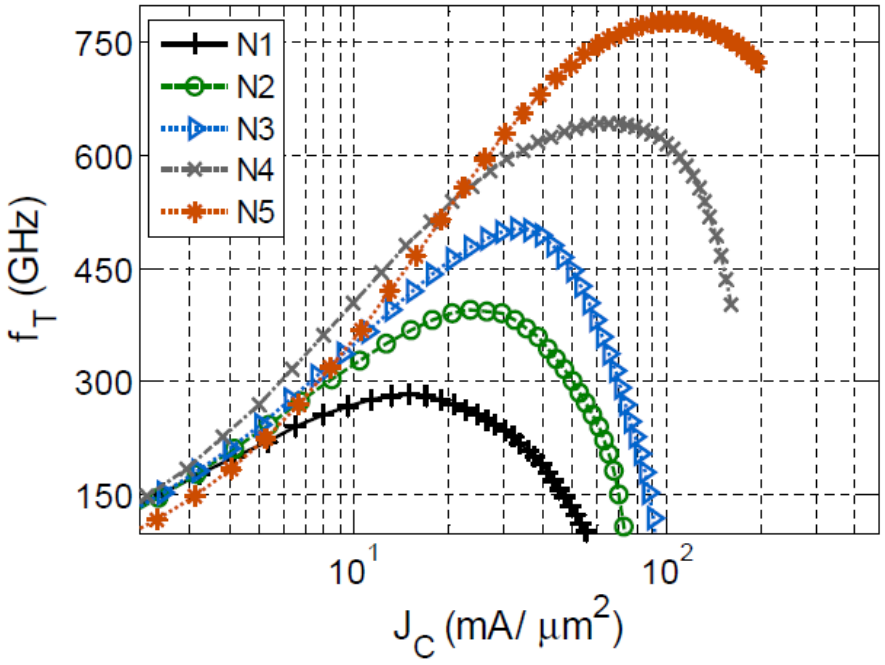
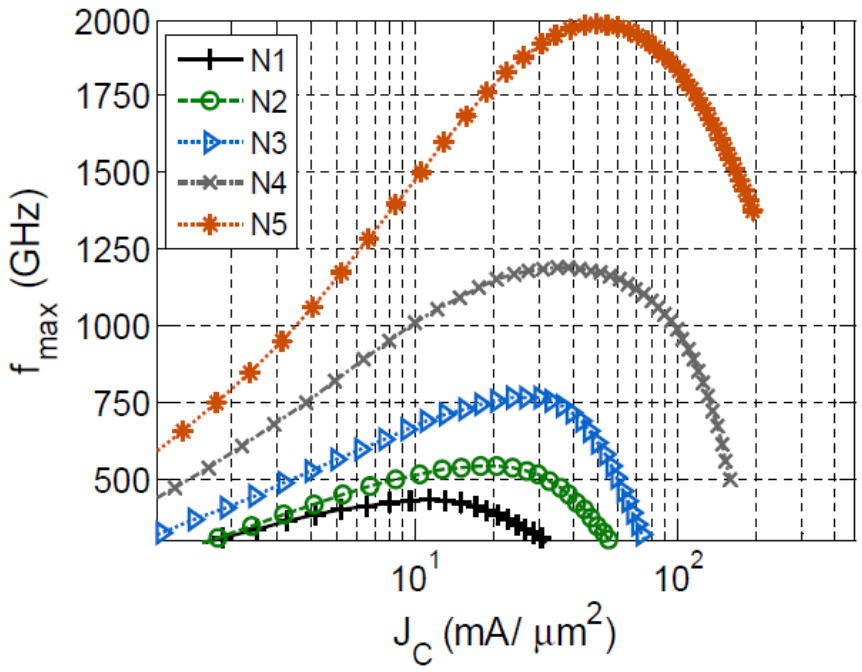
# SiGe Ft / Fmax Technology Trend and predictions

transit frequency *fT* and maximum oscillation frequency *fmax*
... vs. collector current density *JC* for nodes N1 ... N5

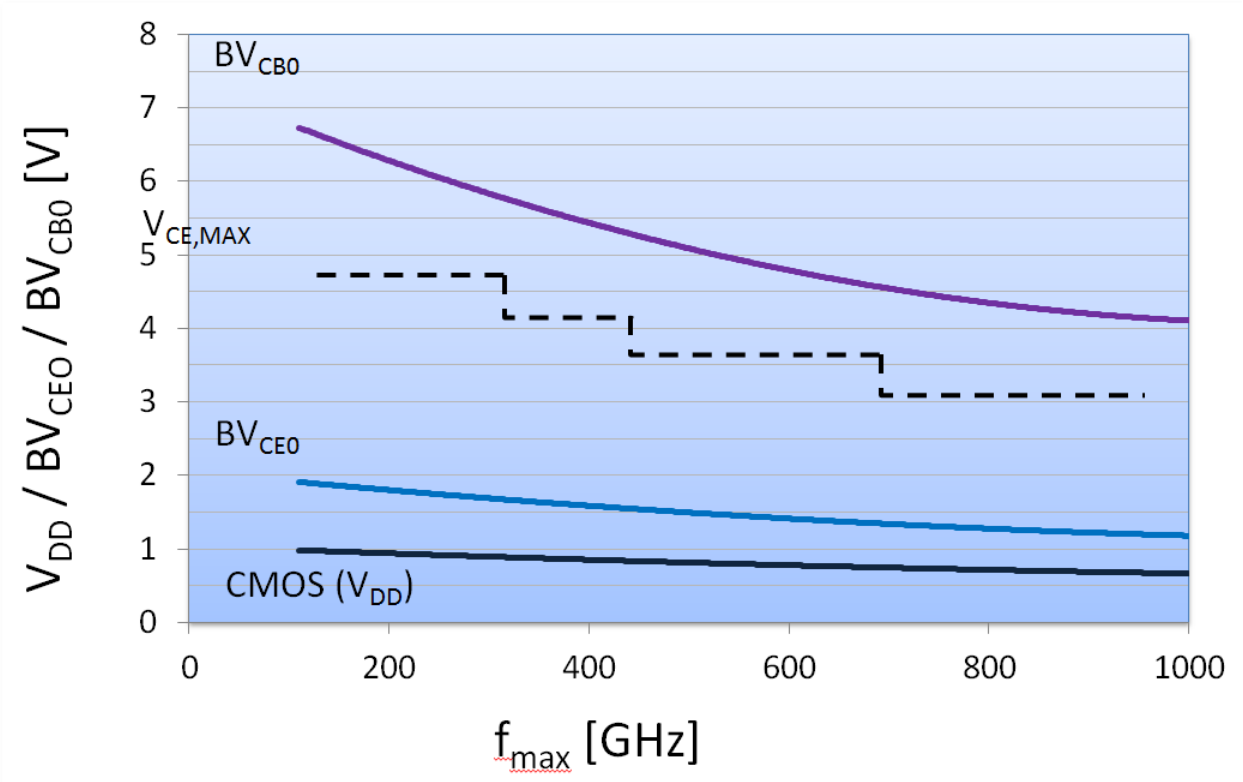



- N1: 130nm, N2: 90nm, N3: 65nm, N4: 40nm, N5: 22nm
- ratio of peak *fmax* values for subsequent generations is about 1.4

**Source:** SiGeC HBT technology roadmap, IMS2015, Phoenix, AZ, 17-22 May, 2015

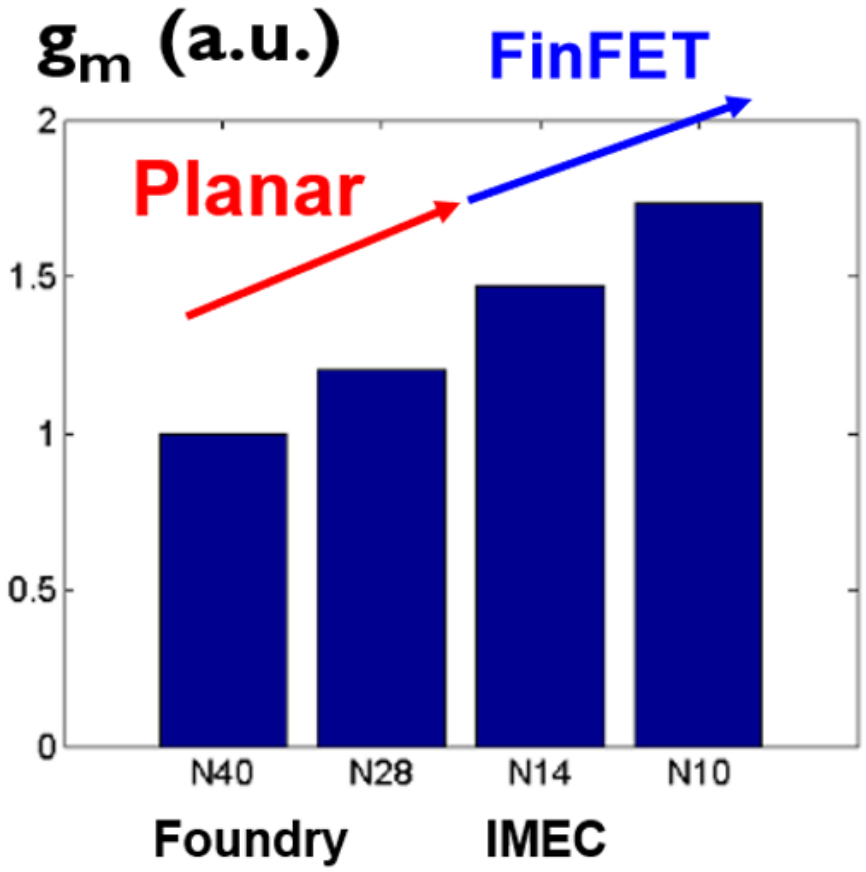
# SiGe $BV_{CE0}$ at high $f_{max}$ trend and predictions

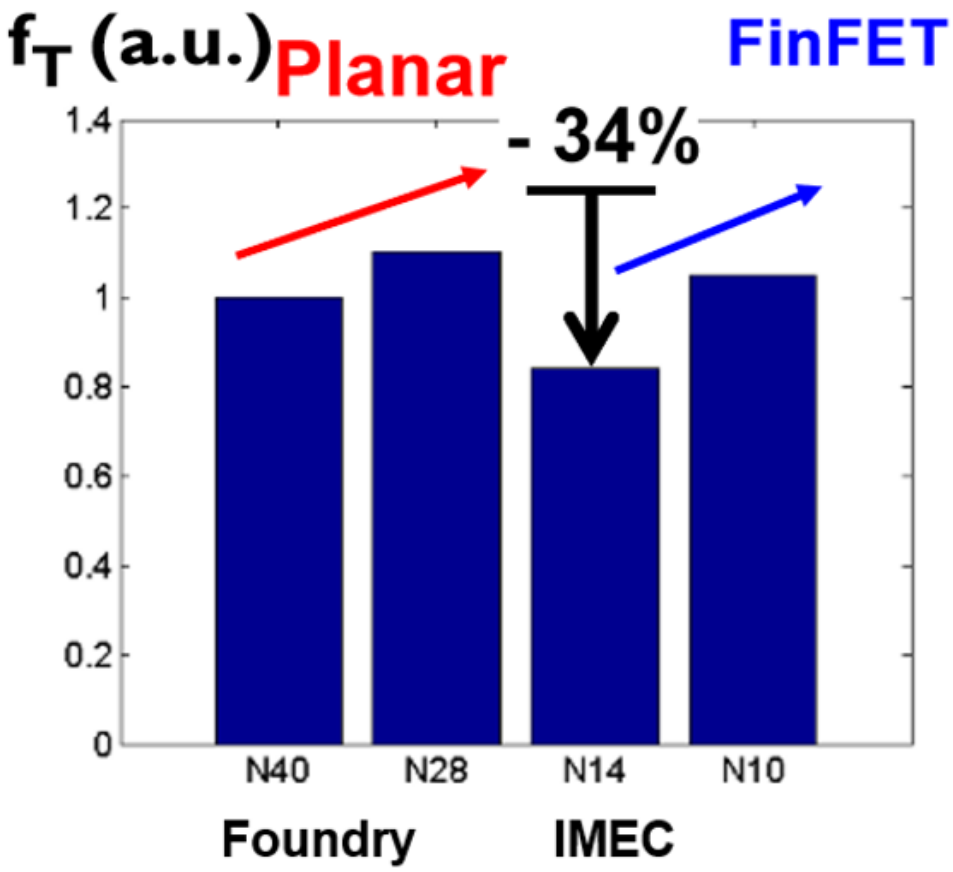



**However $BV_{CES}$ > 5V for the $f_{max}$=250GHz Technology**

**Source:** ITRS RF&AMS Roadmap (Edition 2011)

# FinFET versus FDSOI
# FinFET has more parasitic capacitances

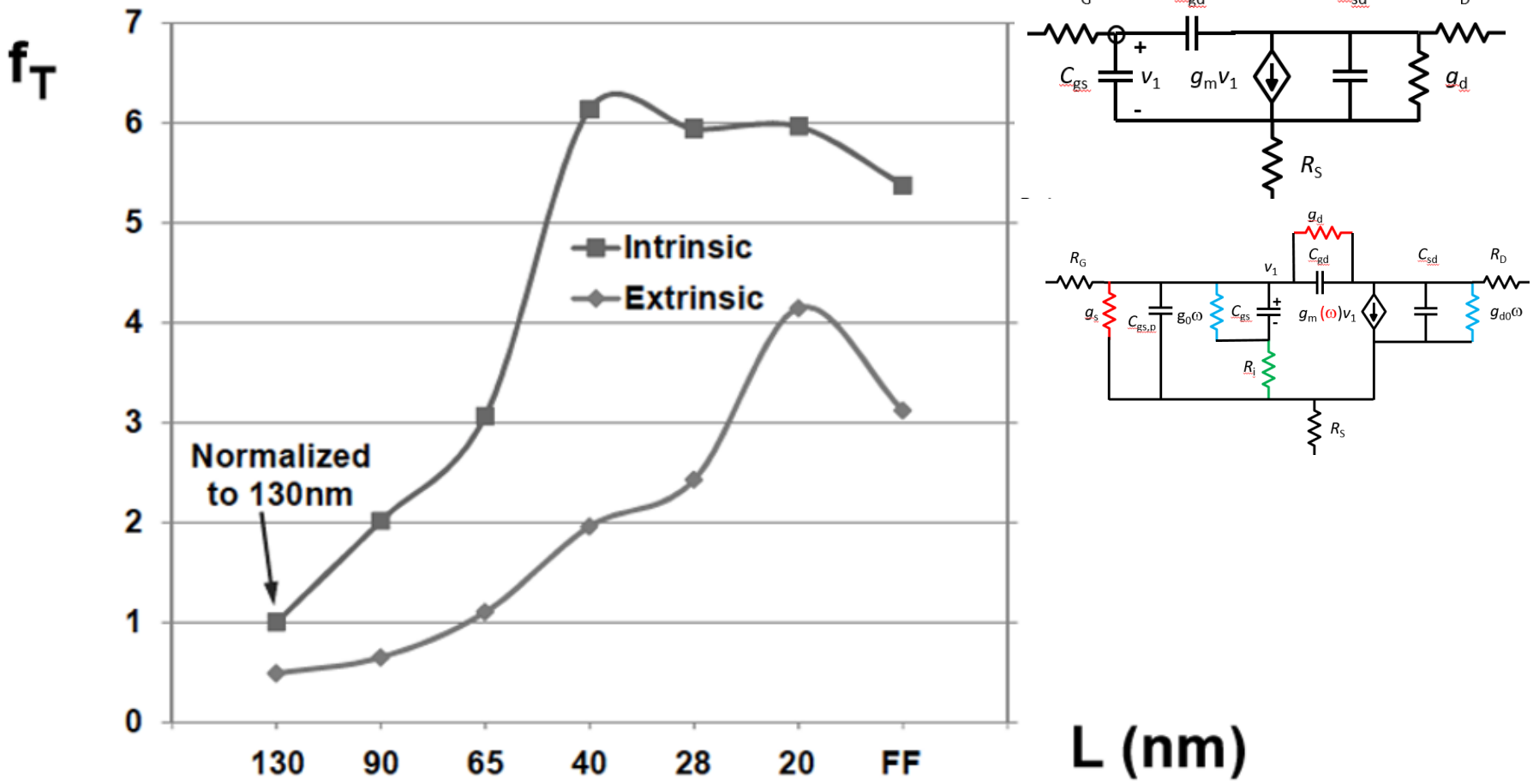



$V_{DS} = V_{DD}$, $V_{GS}$ @ max ($g_m$), $L_G = L_{min}$

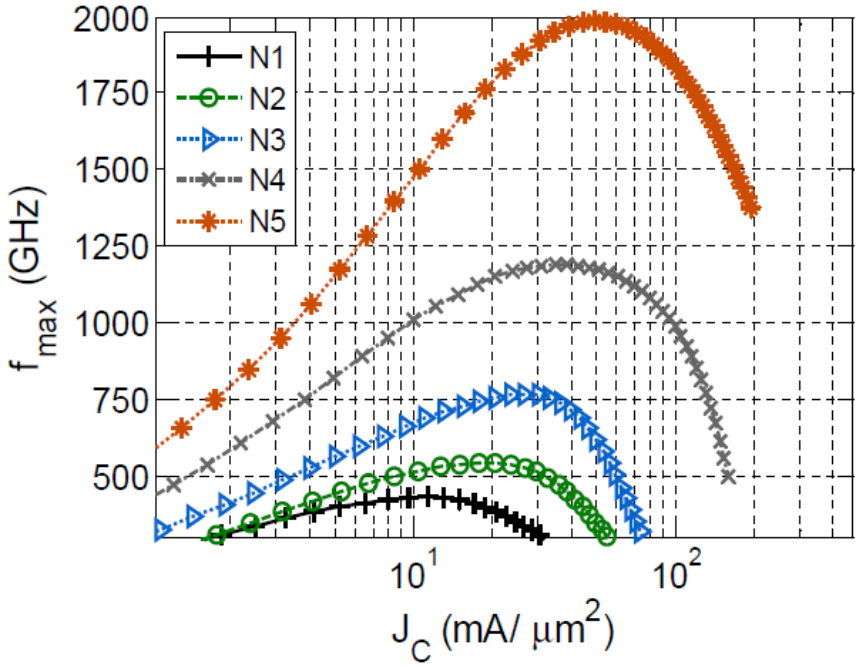
Willy Sansen, ISSCC-2015, plenary presentation

# Speed reduction in FinFETs



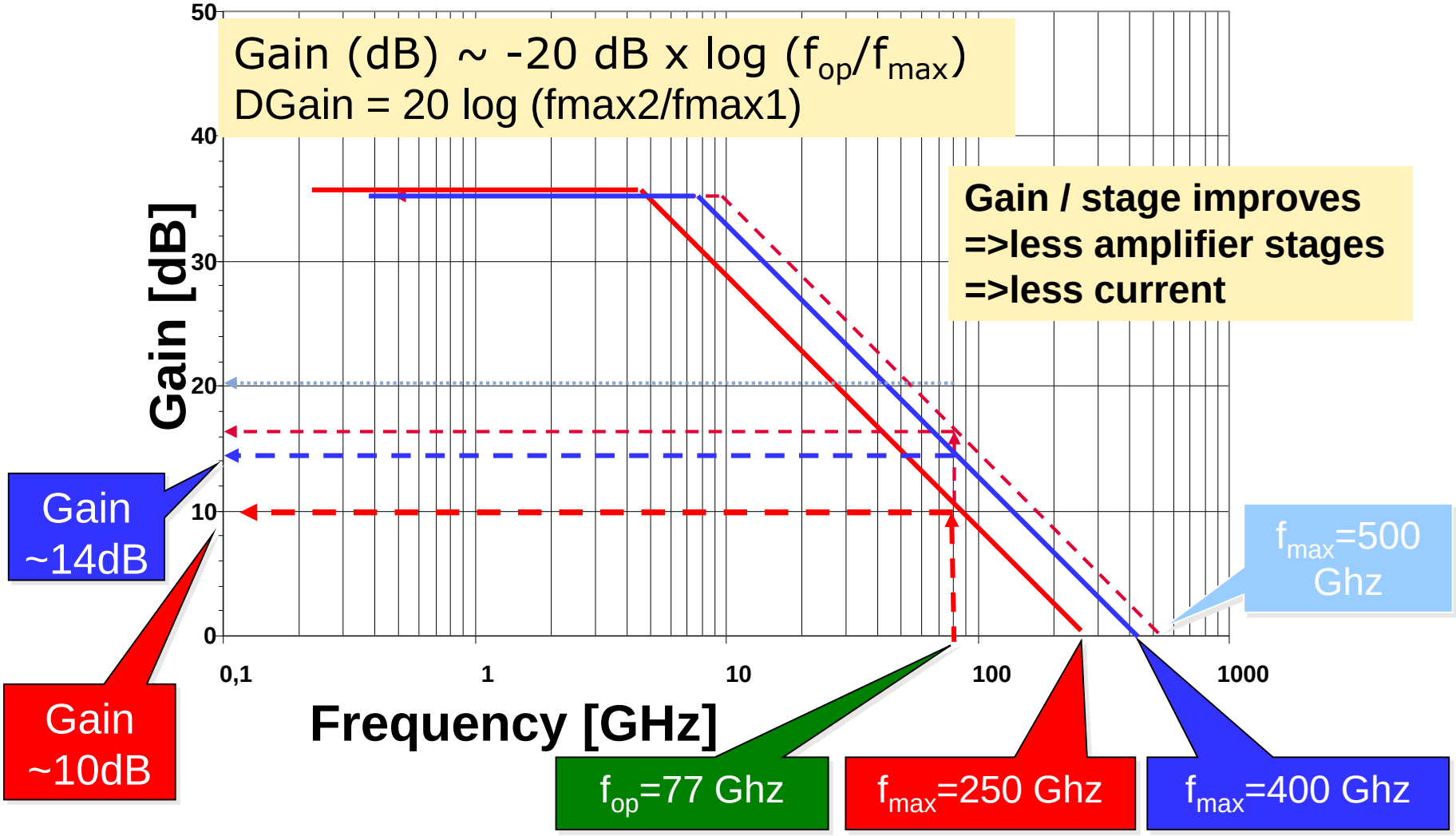

Wakayama, IEDM-2013, 451-454 and Willy Sansen, ISSCC-2015, plenary presentation

# Goldilocks Scaling for SiGe-HBT

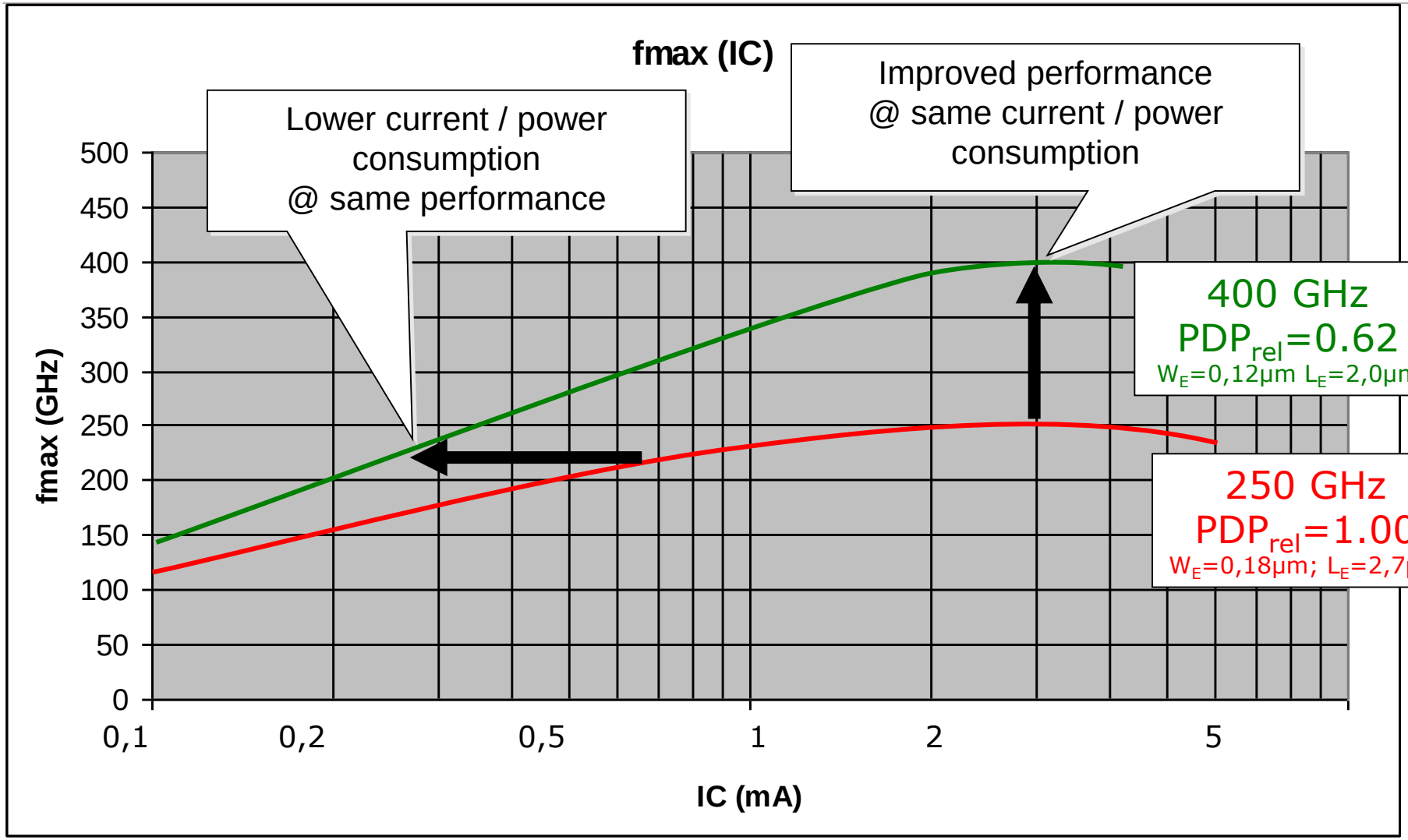



Higher *f*T, higher *f*max, ➔
is the only efficient way to save power
and improve performance SIMULTANEOUSLY
and lower *NFmin*, higher PAE, ...

# Improved Gain/Stage with increased fT/fmax

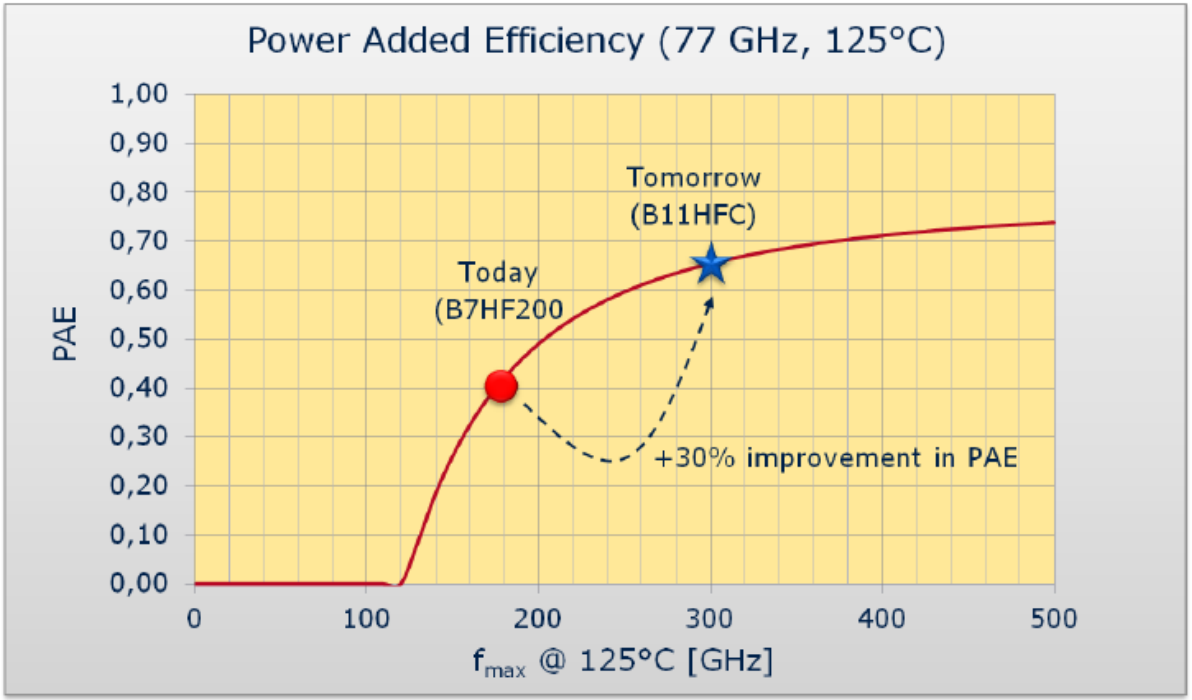


# Why will high $f_T/f_{max}$ save power / current ?




$PDP_{rel}$=relative power*delay product ~ $V_{CC}$ * I / $f_{max}$

# Improved PAE with increased fT and fmax

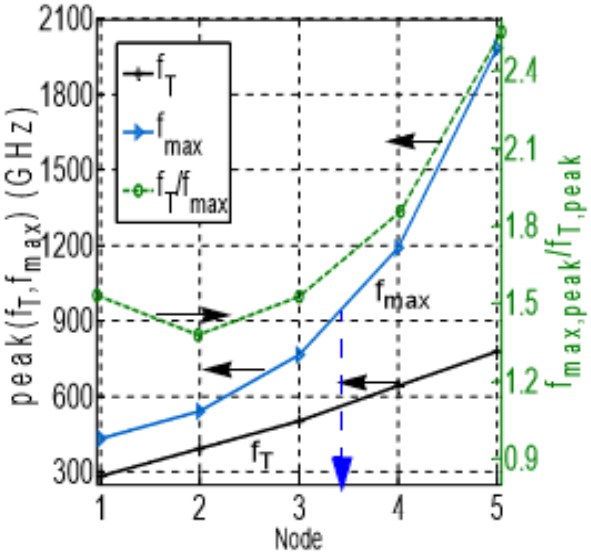



$$PAE = \frac{\pi}{4}\left(1 - \frac{1}{Gain}\right) \approx \frac{\pi}{4}\left(1 - \left[\frac{1}{F_0}\frac{f}{f_{max}}\right]^2\right)$$

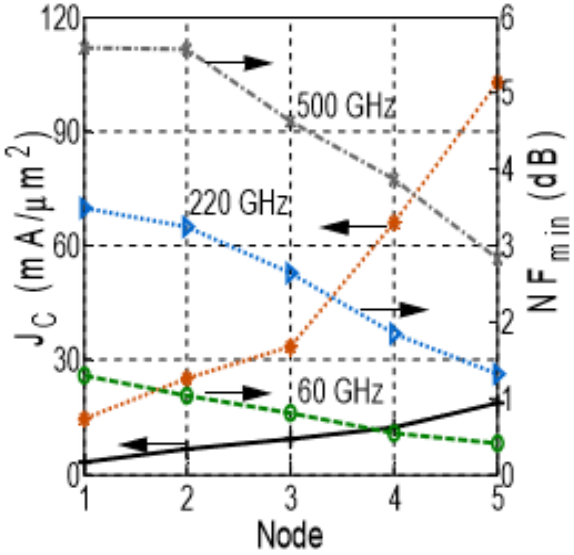
**Source**: J. Scholvin, IEDM 2006

# Evolution of important device related figures of merit

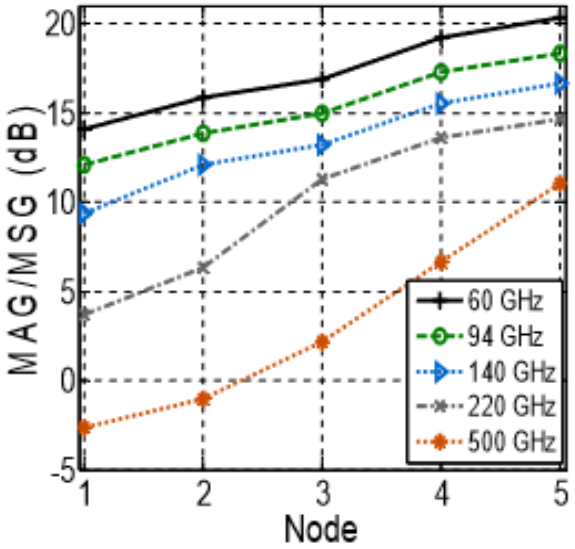
peak $f_T$, $f_{max}$, $f_{max}/f_T$




$NF_{min}$, $J_{C,max}$




power gain

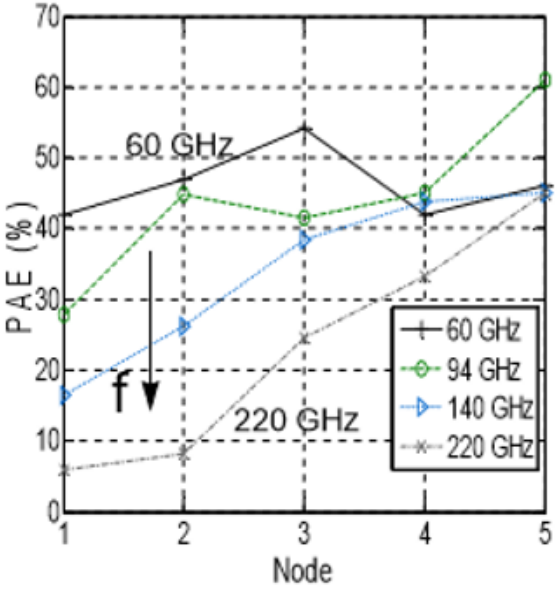



N1: 130nm, N2: 90nm, N3: 65nm, N4: 40nm, N5: 22nm

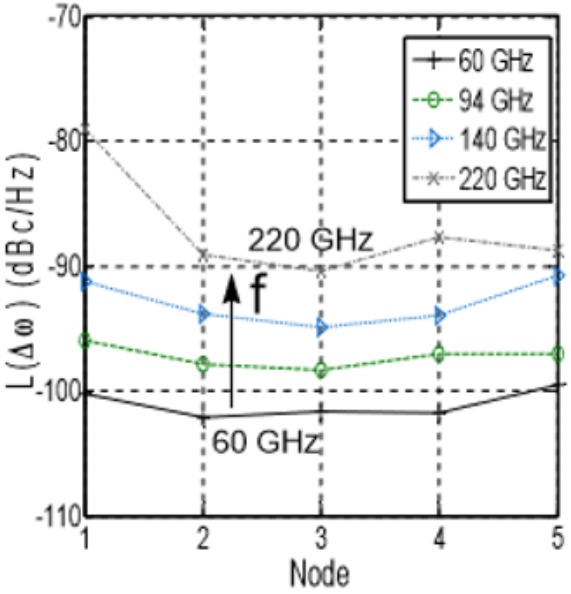
M. Schroeter et al: IMS-2015, WSG-2

# Circuit related performance prediction

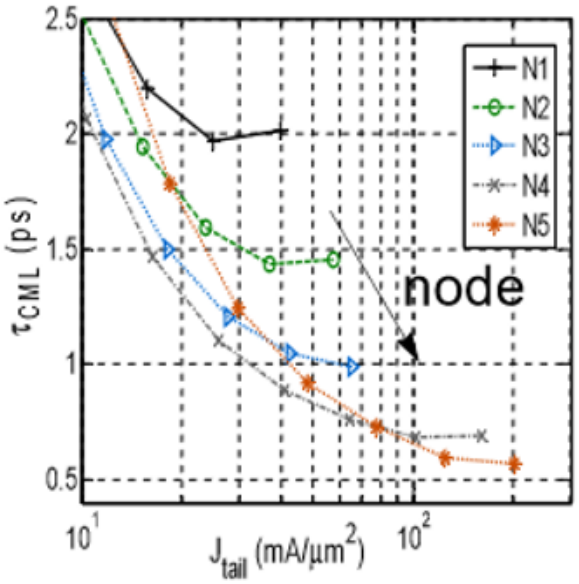
class A/B PA: PAE




VCO: phase noise




CML-RO: delay time




calculated from HICUM/L2 *with all known physical and parasitic effects (incl. self-heating)*

N1: 130nm, N2: 90nm, N3: 65nm, N4: 40nm, N5: 22nm

M. Schroeter et al: IMS-2015, WSG-2

# Technology choice (CMOS versus SiGe-BiCMOS) mm-Wave RF-beamformers - Comparison Table

| | Infineon | [1] Tokyo IT | [2] Qualcomm | [3] IBM | [4] UCSD |
|---|---|---|---|---|---|
| **Technology** | SiGe 130nm | CMOS 65nm | CMOS 28nm | SiGe 130nm | SiGe 180nm |
| **Freq. [GHz]** | 24.25-30.5 | 28 (n257) | 28 (n257) | 27-29 | 28-32 |
| **Channels** | 4 | 4 (4xH-BF, 4xV-BF) | 24x TRX | 16/pol (16xH/16xV-TRX) | 4 (4xH-BF, 4xV-BF) |
| **Area [mm$^2$]** | 19.4 | 12 | 27.8 | 165.9 | 23 |
| **Package** | eWLB | – | Flipped on PCB | Laminate | Flipped on PCB |
| **RX $P_{dc}$ [W]** | 1.6 (0.4/path) | 0.6 (0.112/path) | 0.042/path | 3.3/pol (0.206/path) | 0.15/path |
| **TX $P_{dc}$ [W]** | 1.8 (0.45 @$P_{1dB}$/path) | 1.2 (0.252 @11.3 dBm/path) | 0.119 @11 dBm/path | 4.6/pol (0.319 @16.4dBm/path) | 0.22/path |
| **RX NF [dB]** | 4 | 4.2 | 4.4 – 4.7 | 6 (Front-end) | 4.8 |
| **BITE** | YES | NO | NO | NO | NO |

# Landscape of 5G SoCs

| | | Qualcomm | Samsung | Intel | Mediatek | HiSilcon | UNISoC |
|---|---|---|---|---|---|---|---|
| | | X55 | Exynos 5100 | XMM8160 | M70 | Balong 5000 | IVY510 |
| **Availability** | | 2H 2019 | 1H 2019 | 1H 2010 | 2H 2019 | 2H 2019 | 2H 2019 |
| **CMOS Node** | | 7 nm | 10 nm | 10 nm | 12 nm | 7 nm | 12 nm |
| **Modem** | Modes | 5G/4G/3G/2G | 5G/4G/3G/2G | 5G/4G/3G/2G | 5G/4G/3G/2G | 5G/4G/3G/2G | 5G/4G/3G/2G |
| | Radio | Dual | Dual | Dual | Dual | Dual | Dual |
| | | TDD/FDD | TDD/FDD | TDD/FDD | TDD/FDD | TDD/FDD | TDD/FDD |
| **3GPP** | | NSA/SA | NSA/SA | NSA/SA | NSA/SA | NSA/SA | NSA/SA |
| **mmWave** | CA | 8 x 100MHz | 8 x 100MHz | 8 x 100MHz | ? | 8 x 100MHz | ? |
| **Sub-6 GHz** | CA | 2 x 100MHz | ? x 100MHz | 2 x 100MHz | 2 x 100MHz | 2 x 100MHz | ? X 100MHz |
| **LTE Support** | | CAT-22 | CAT-10 | CAT-22 | CAT-12 | CAT-19 | CAT-12 |
| | CA | 7 | 8 | 8 | 3 + | 5 | 3 + |
| | Mod | 1024 QAM | 256 QAM | 256 QAM | 256 QAM | 256 QAM | 256 QAM |
| | Layers | 24 | 16 | 24 | ? | 16 | ? |
| | MIMO | 4x4, FD-MIMO | 4x4, FD-MIMO | 4x4 | 4x4 | 4x4 | |

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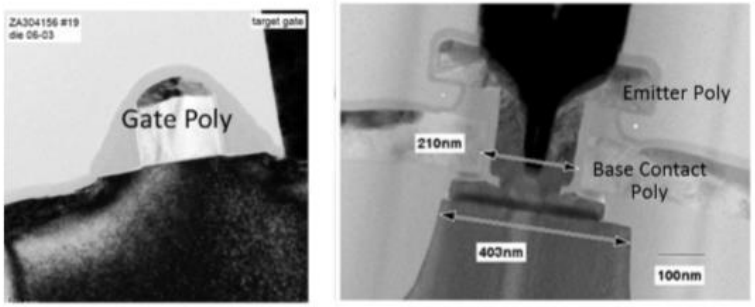
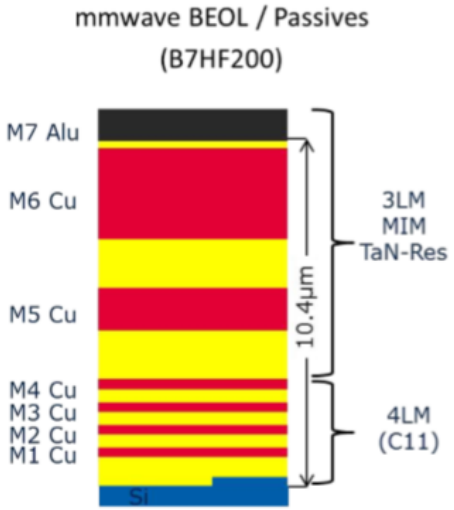
# B11HFC : 130 nm BiCMOS

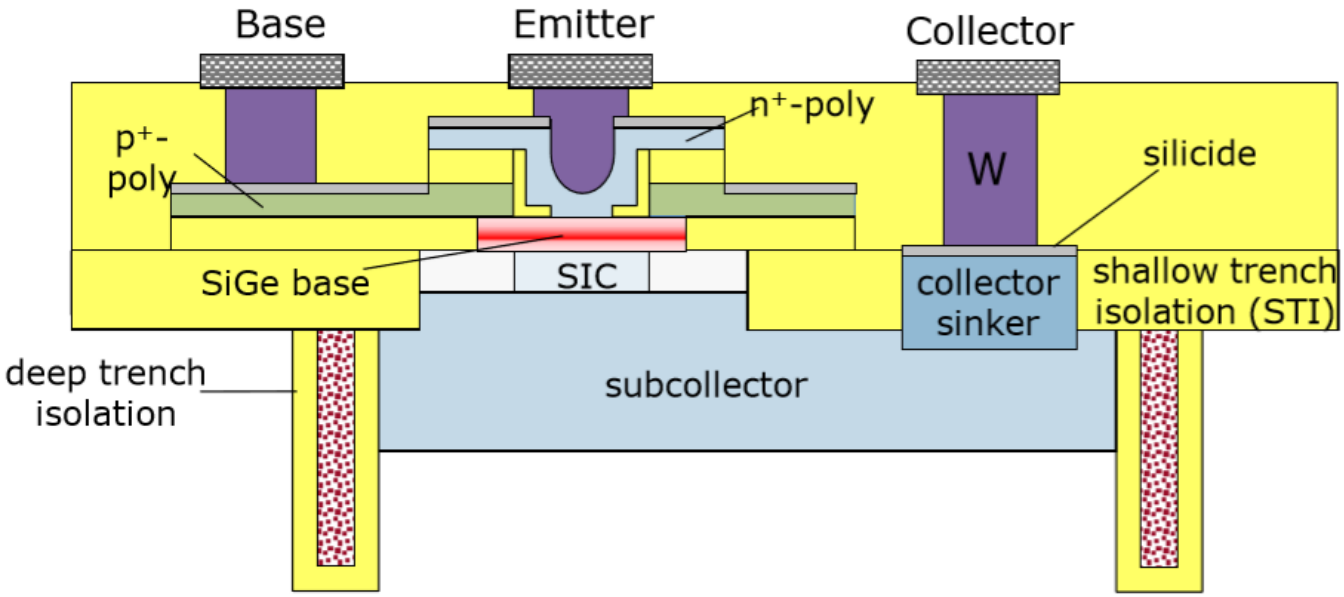
130nm MOSFETs (C11) & Scaled SiGe HBTs DOT5/7 &




- Mature 130 nm CMOS node
- High-speed SiGe HBTs with fT = 250 GHz , fmax = 400 GHz
- 7 layer metallization with MIM capacitor, metal resistor and laser fuse
- Qualified in 2017

# DPSA Configuration of SiGe HBT Used in Current Production



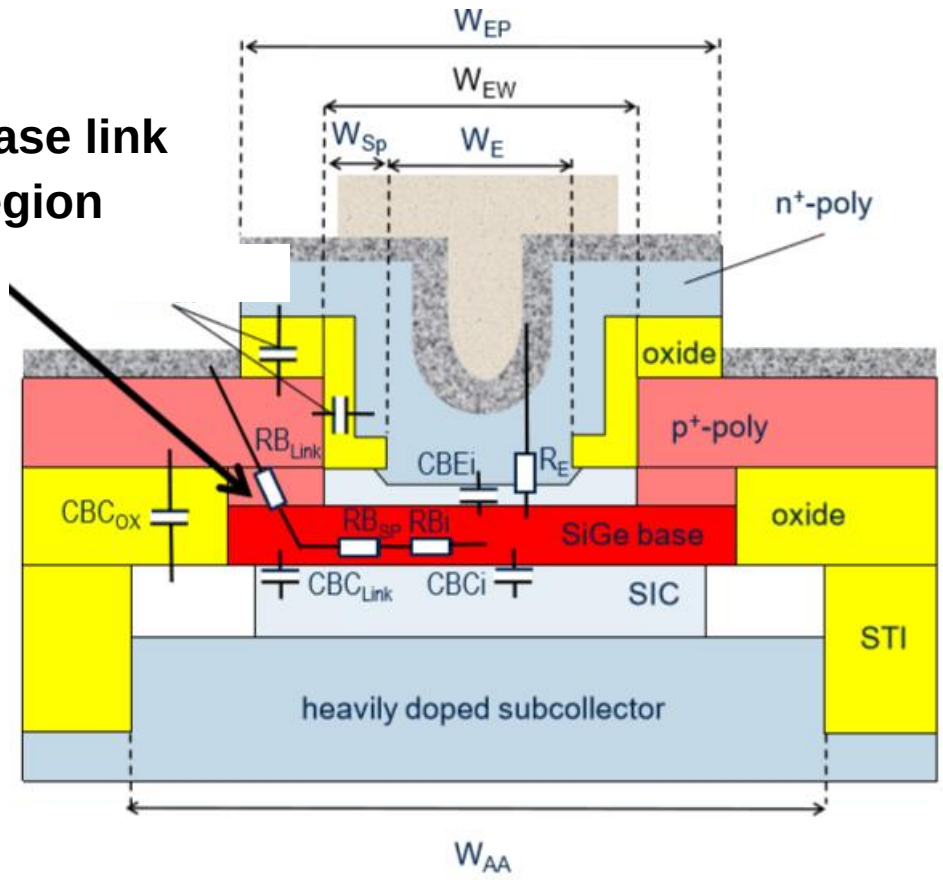

- E/B configuration: Double Polysilicon Self-Aligned with Selectively Grown Epitaxial Base Link (DPSA-SEG)
- Transistor isolation: Deep trench (DT) and shallow trench isolation (STI)

# Challenge to achieve THz performance

## Process flow for base link region to be optimized

Schematic cross section of EB region and electrical parasitic elements

**Base link region**

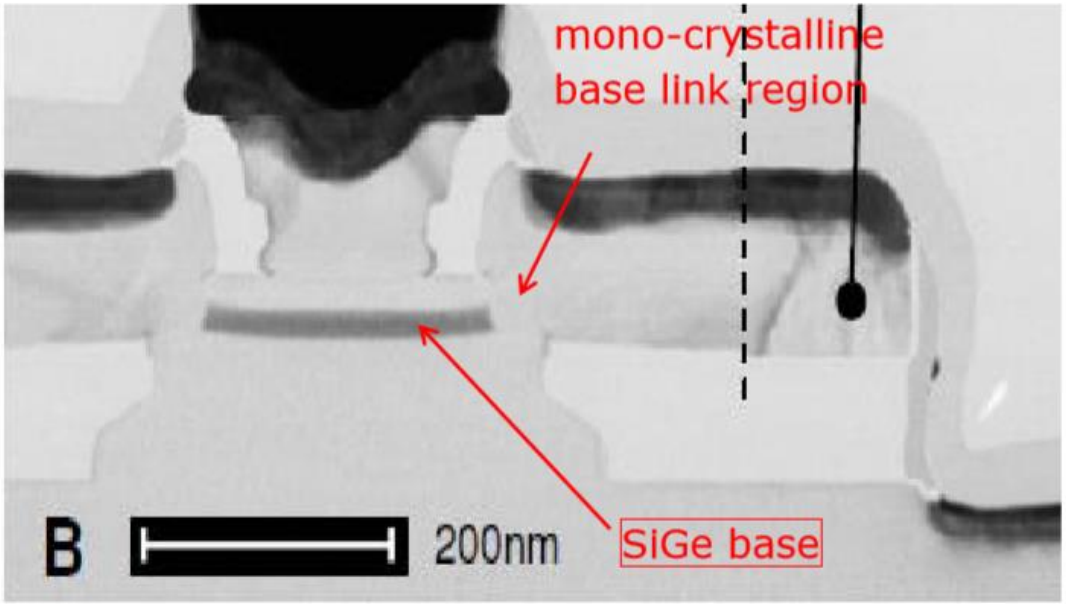



- Links active NPN base and p+-polysilicon base electrodes
- Formed during selective epitaxial growth
- This is a major limiting factor for $f_{max}$ (high RB)

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_{BC}}}$$

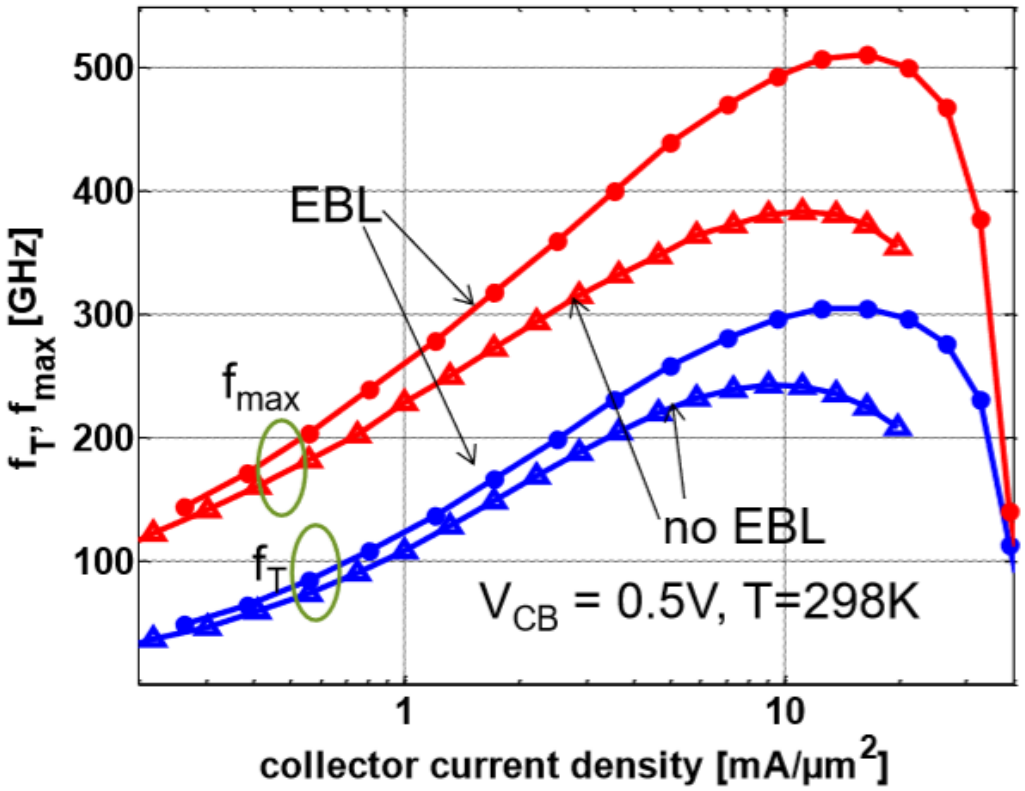
# HBT with improved $f_T/f_{max}$ by novel device architecture

## HBT with Epitaxial Grown Base Link (IHP)



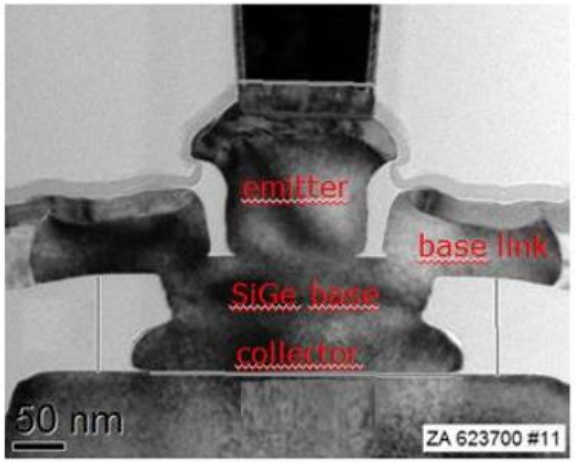

- Basic idea: de-couple SiGe base and base link deposition
- Highly doped base link epitaxy: low $R_B$
- No base link anneal necessary: steep base profile, high $f_T$

# RF Characteristics DPSA-SEG vs. EBL concept

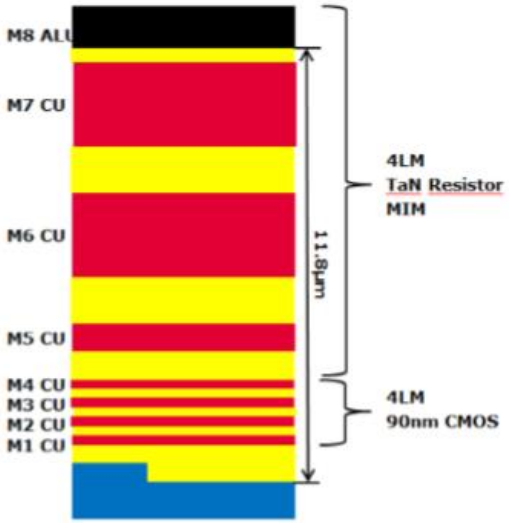



Novel EBL device architecture offers low base link resistance and key performance metrics like tD ~ 1.7ps and fmax ~ 600 GHz and is a base for further scaling

# Infineon‘s next generation 600 GHz BiCMOS technology








- SiGe HBT with epitaxial base link
- Target values $f_T$ = 300GHz, $f_{max}$ = 600GHz, effective emitter window < 100nm
- 90nm CMOS:  1.9nm thin GOX / 5.8nm thick GOX
- 8 layer metallization with TaN resistor, MIM

# BiCMOS Integration Issues

- CMOS devices should not be changed (reuse CMOS IP, ROM, SRAM, …)

ISSUES:

- MOS thermal steps deteriorate HBT performance
- EBL HBT and fineline CMOS technology:
  - Substrate orientation for best HBT performance & yield different from standard CMOS
  - Different optimal thermal budgets for HBT and CMOS fabrication

SOLUTION:

- Removal of HBT stack from CMOS regions
- Removal of CMOS spacers from bipolar areas
- .....

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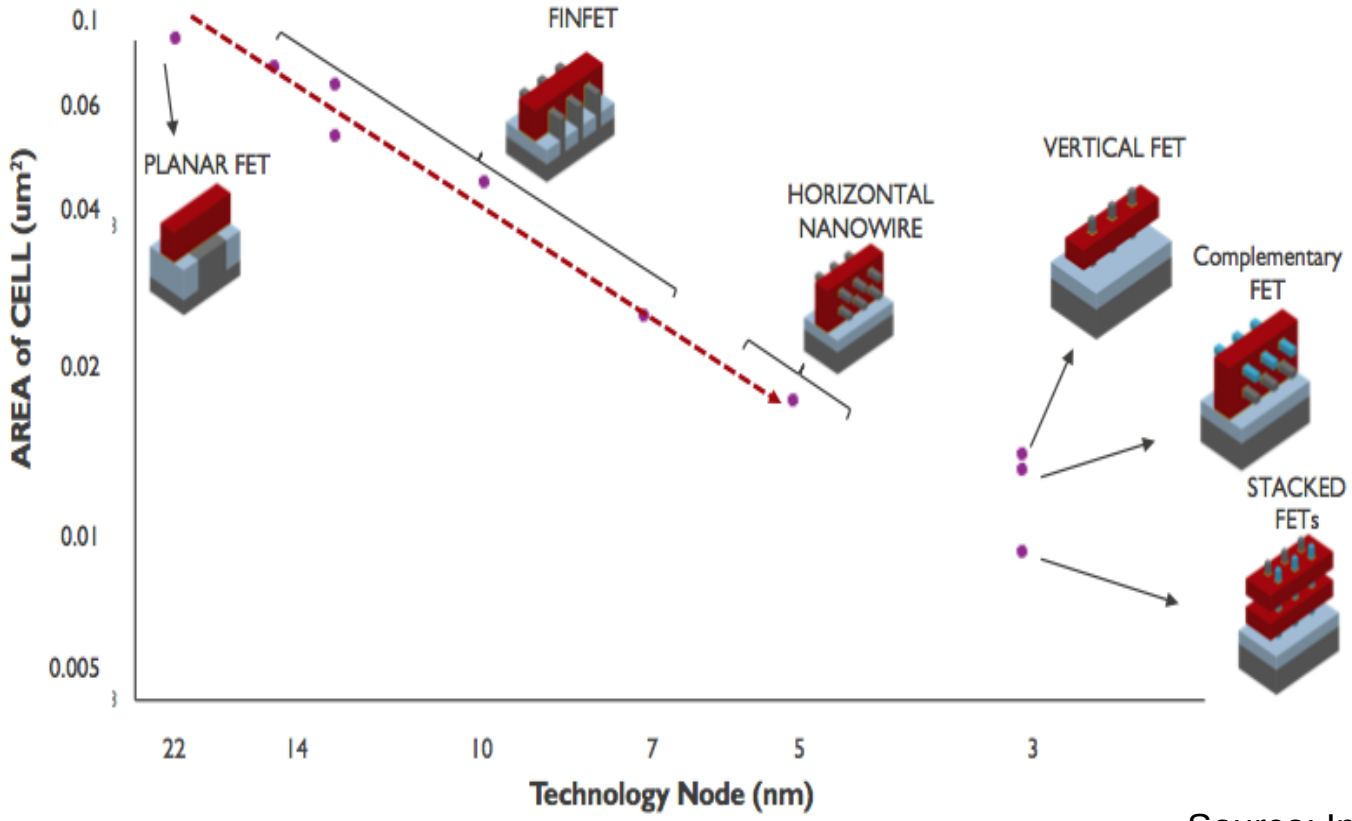
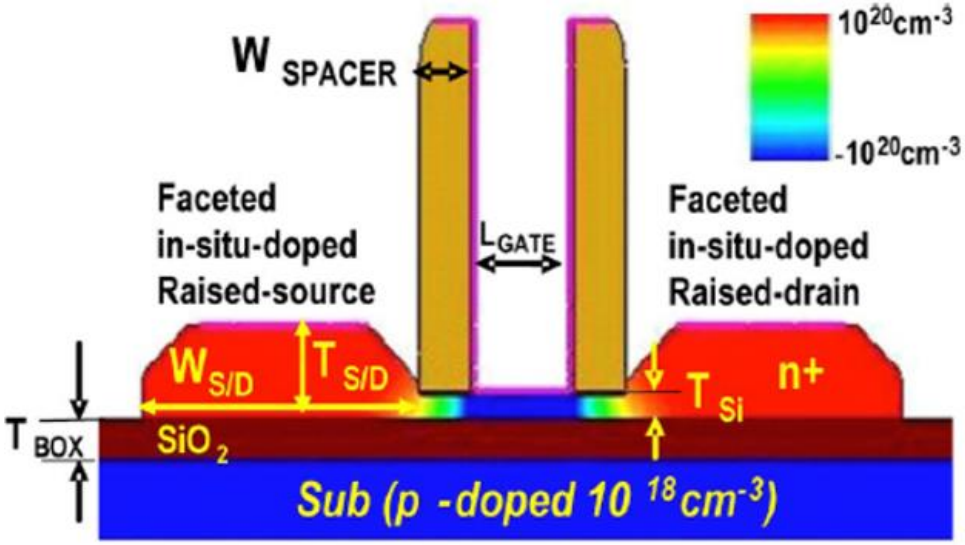
# Next-gen transistor architectures



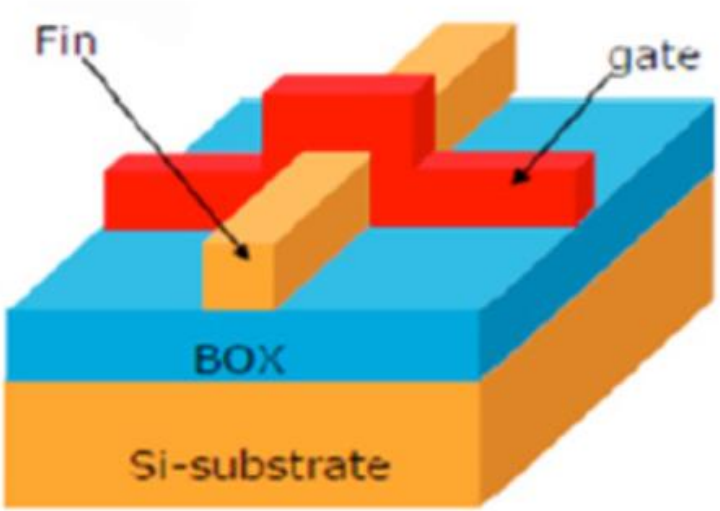

Source: Imec/ISS

Roadmap foggy below 7nm: high mobility FinFET (Germanium), gate all around, vertical nanowires, Tunnel-FETs, Quantum well devices

# Downscaling planar CMOS: deadend street




**FD-SOI CMOS**



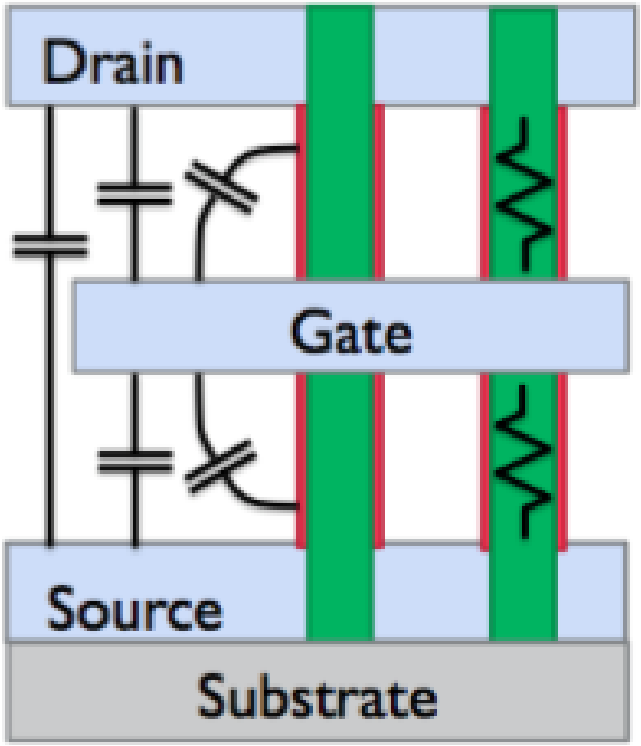

**SOI FinFET**

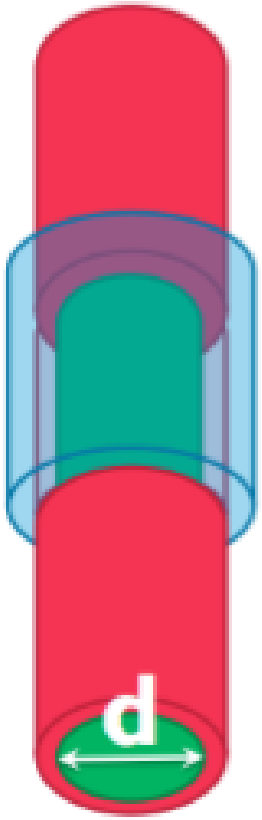
**Shin, ..., Tr ED June 2010, 1301-1309**
**Jacquet, ..., JSSC Apr.14, 812-824**

- Short-channel effects ? FinFET ? Towards 5nm ?
- FDSOI is still planar – later towards FinFET ?

Willy Sansen, ISSCC-2015, plenary presentation

# Vertical FET - Nanowires



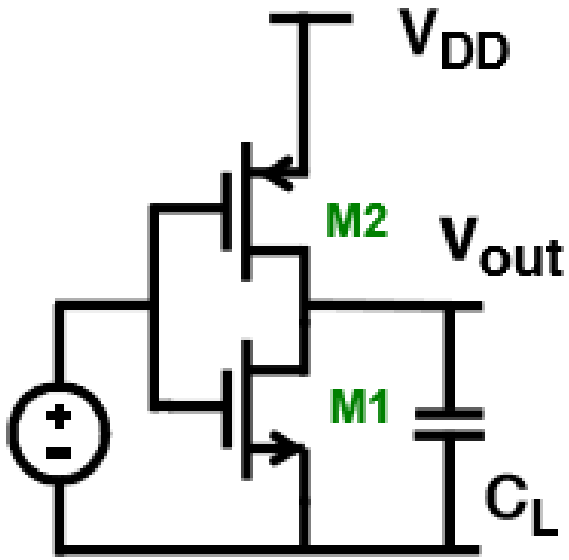

- Nominal device:
  d = 8 nm
  L = 15 nm
  EOT = 0.6 nm
  NW Pitch = 17 nm
- 
- VDD = 0.5 V
  SSSAT = 61.1 mV/dec
  DIBL = 22.8 mV/V

N. Collaert, “CMOS Nanoelectronics, Pan Stanford Publishing

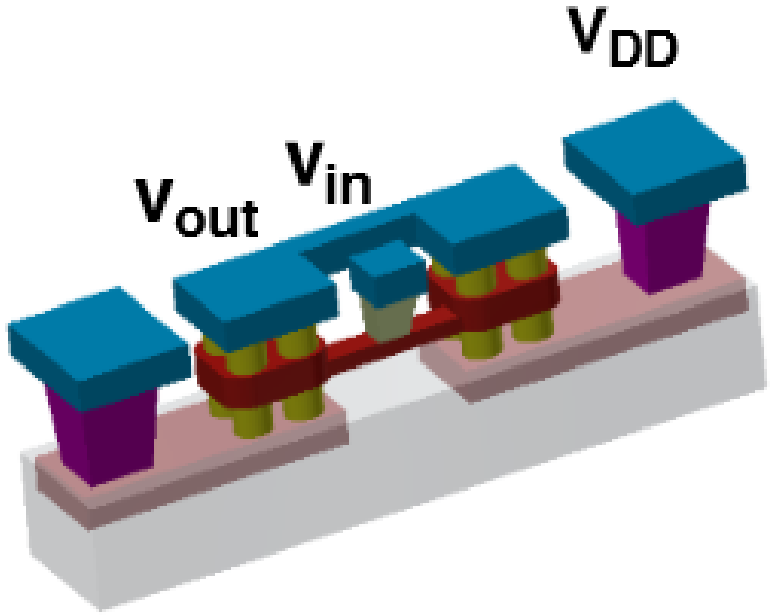
IMEC ITF 2014

Willy Sansen, ISSCC-2015, plenary presentation

# CMOS Inverter with 7 nm V-FETs

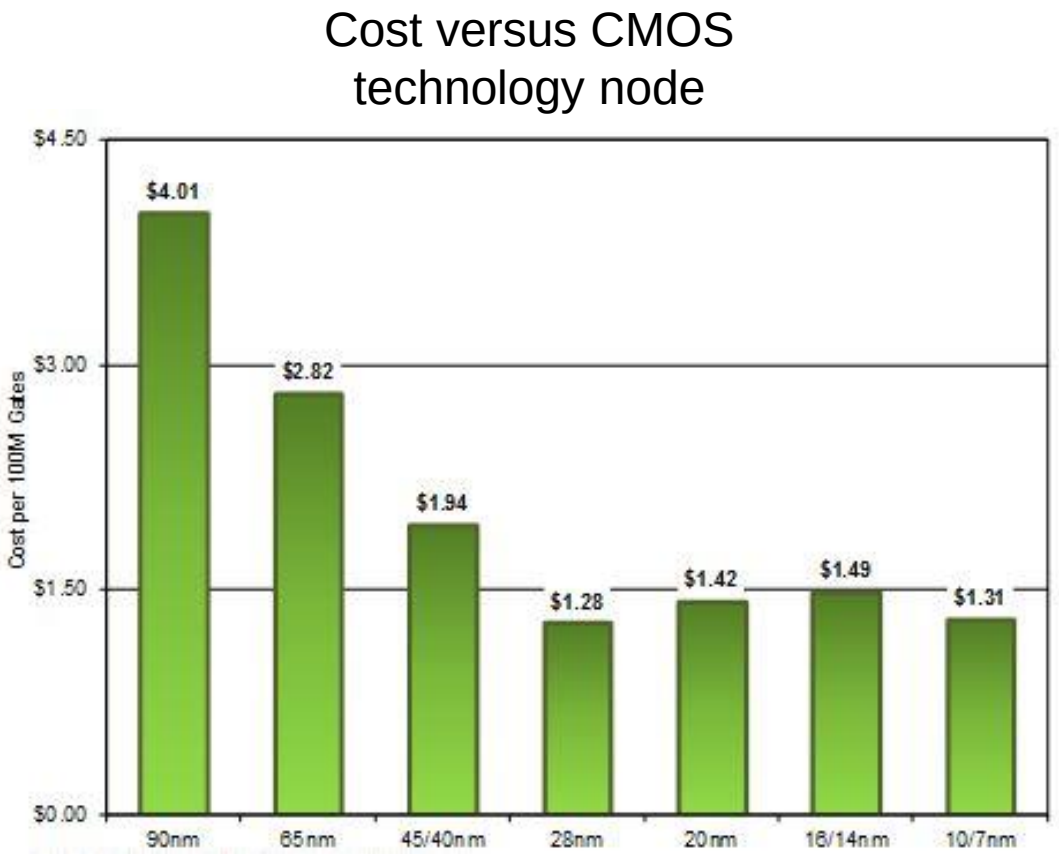



CMOS invertor

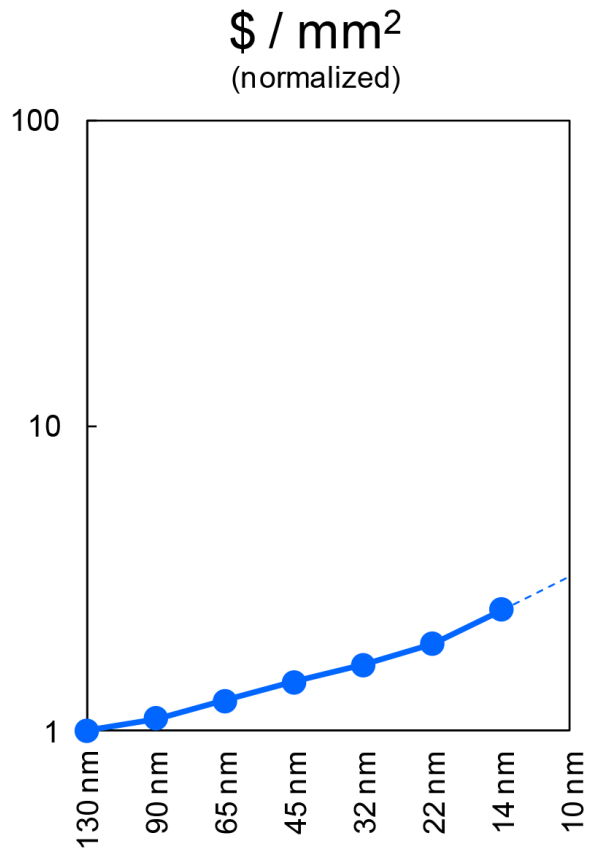



Willy Sansen, ISSCC-2015, plenary presentation

# Cost versus CMOS technology node
# Cost per Transistor

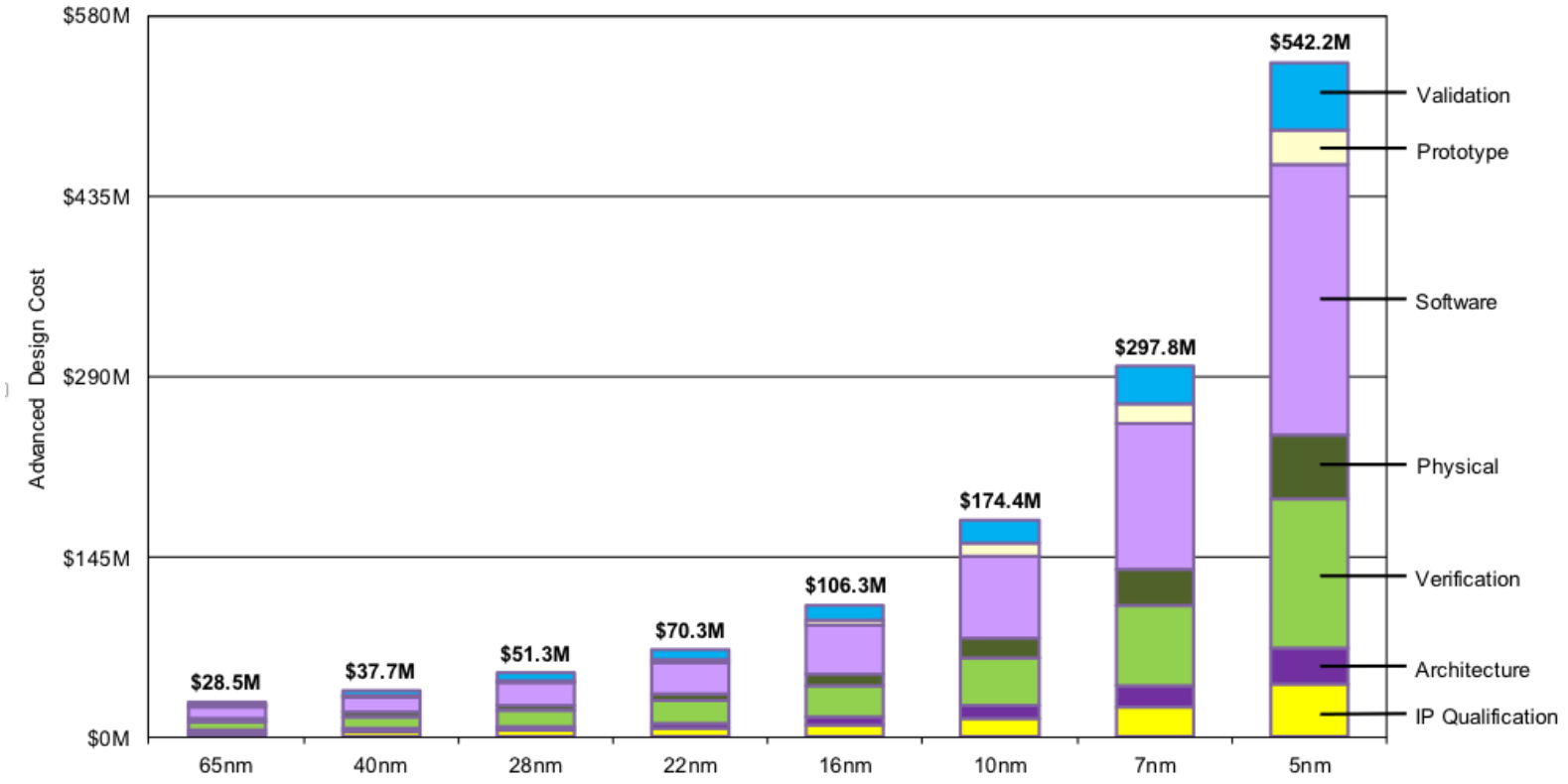



Source: International Business Strategies, Inc. 2015




Source: Intel – Embargo until 8-11-14, 9 am PDT

# IC design costs




Source: IBS 2018

# H2020 INSIGHT

INSIGHT

INTEGRATION OF III-V NANOWIRE SEMICONDUCTORS FOR NEXT GENERATION HIGH PERFORMANCE CMOS SOC TECHNOLOGIES

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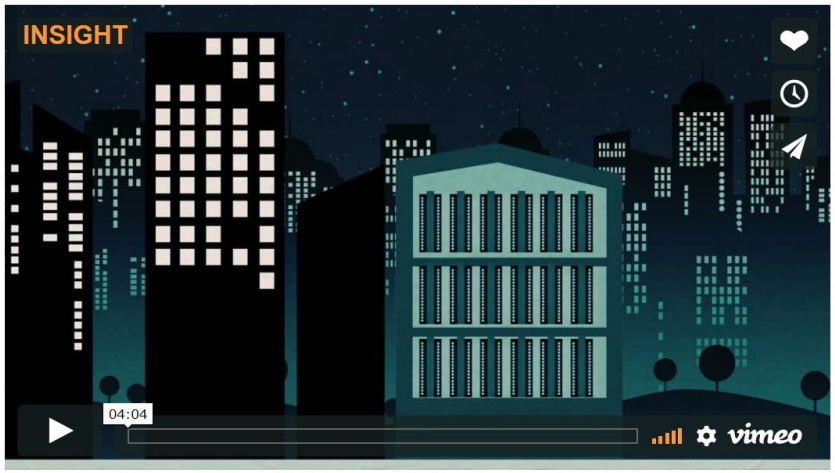
- Integration of III-V Nanowire Semiconductors for next Generation High Performance CMOS SOC Technologies

- Vision:
  *„…to use III-V nanowire CMOS technology for millimeter-wave applications in a System-on-Chip approach, combining RF- & logic on one Si chip. Applications for logic at the 10 nm node and beyond are foreseen.“*

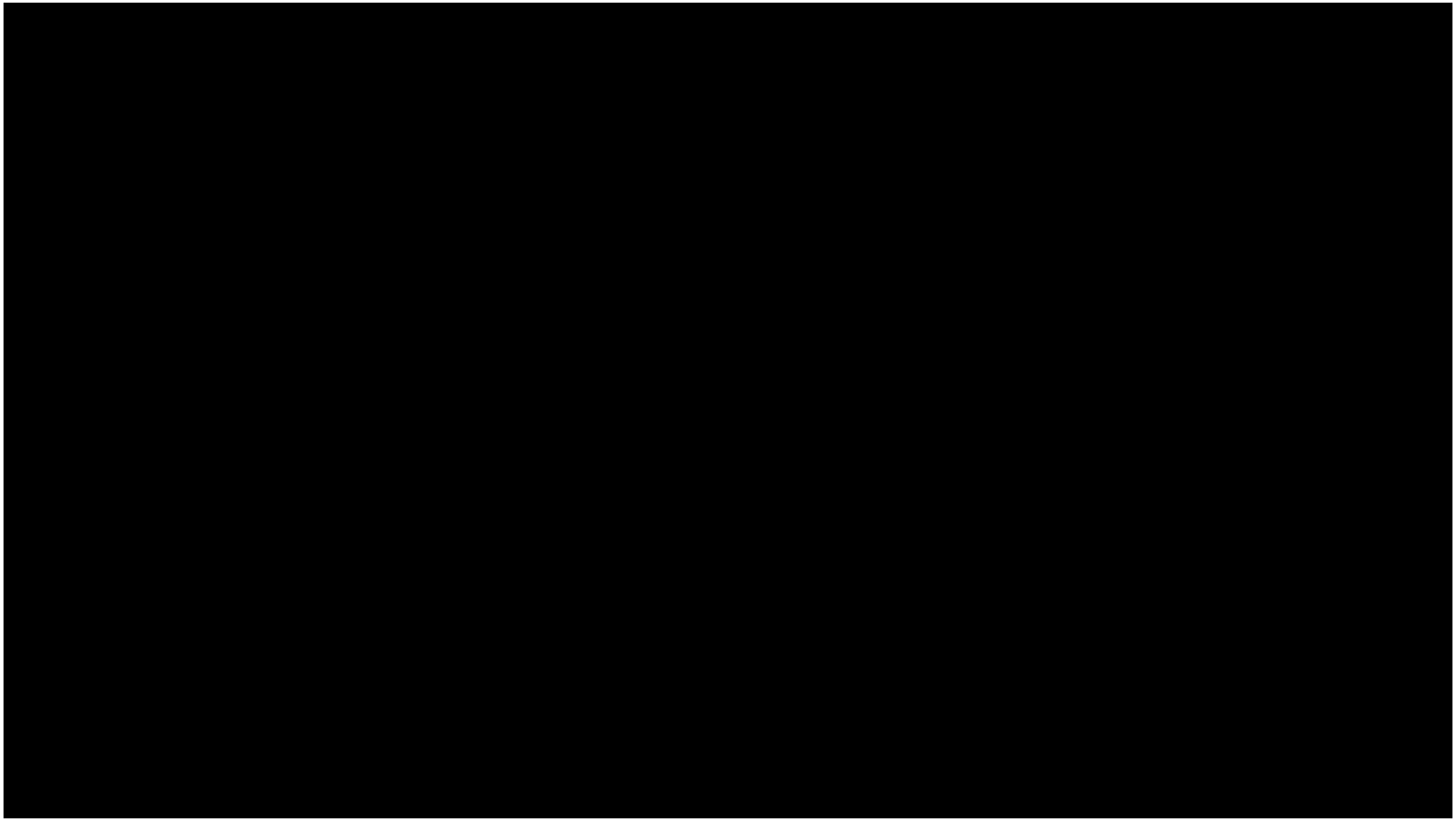



http://www.insight-h2020.eu/

INSIGHT video:

https://www.youtube.com/watch?v=UthfXTO9DFM&feature=youtu.be

# H2020 INSIGHT



# OUTLINE

- Introduction
  - Market trends and RF requirements
- Technology Roadmap and Moore's Law
  - ITRS (IRDS)
  - CMOS / FinFET / FDSOI / SiGe-BiCMOS
  - SCALING
- SiGe-BiCMOS process flow
- Next generation transistor architectures (new technologies)
- Summary

# Conclusions

- Push towards THz frequencies
  - A lot phenomena in solids, liquids and gases occur in the THz domain
  - Where to find the spectrum for 1 Tb/s
- Scaling and push for higher *f*T and *fmax is the* only efficient way to save power and improve performance SIMULTANEOUSLY
- SiGe-HBT: $f_{max}$ = 2 THz achievable by novel device architecture and scaling to 20nm
- CMOS speed is saturationg $f_T/f_{max}$ limited to < 500 GHz
  HF circuit performance scaling already peaked at 28nm
- Vision *to use III-V nanowire CMOS technology for millimeter-wave applications*
- Below 28nm exponential increase in cost for production and design effort

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