technologies

Microwave Characterization Center

contact@mc2-technologies.com www.mc2-technologies.com +33 3 20 04 55 67

Chalmers Winter School

-

GaN Power amplifiers

January 16th, 2020

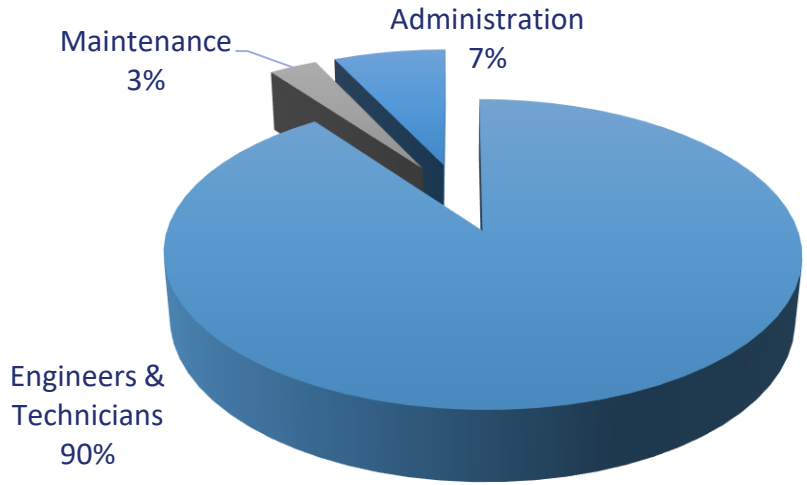
MC2 technologies

SUMMARY :

MC2-Technologies Figures

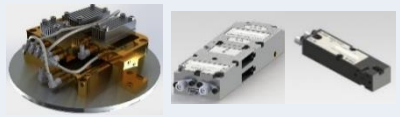
- Microwave Characterization Center (MC2)
- Spinoff from IEMN laboratory, Lille-métropole
- Created in 2004 by:
  - Nicolas Vellas, Ph.D (CEO)
  - Christophe Gaquière, Pr. (CTO)
- > 50 employees
- Involved in several European R&D projects :
  - H2020 Spiders
  - H2020 ALADIN
  - H2020 GRACE
- Turnover 2019: 8M€

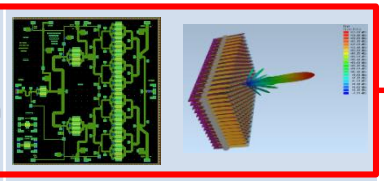
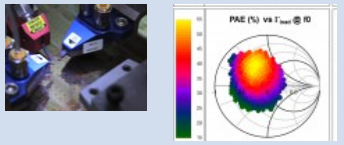
- New facilities in 2020 !



MC2-Technologies Activities

Security Products	
MM-Imager	
UAV Scrambler	
Microwave shield meter	

Microwave Products	
Amplifiers	
TR modules mmW	
Pulsed IV system 1000V/20A	
Efuse, Bias tee, Kit SMM	

Services	
Design MMIC Hybrid & antenna	
Prototyping	
Characterization	
Reliability tests	

- GaAs and GaN MMIC (PA, LNA, Mixers…)
- OMMIC, UMS, WIN processes

Permanent R&D Program on products and services (H2020, ANR)

OMMIC GaN Processes

OMMIC Processes

Process	ED02AH	D01PH	D01MH	D007IH	D01GH	D006GH
Technology	GaAs p-Hemt	GaAs p-Hemt	GaAs m-Hemt	GaAs m-Hemt	GaN on Si/SiC	GaN on Si/SiC
Status	Production	Production	Production	Production	Preproduction	Development
Space Grade	Space Qualified	Space Qualified	Space Qualified	In 2020	In 2020	-
Gate Length (µm)	0.18	0.135	0.125	0.07	0.1	0.06
Wafer Size (")	3	3	3	3	3	3
Thinkness (µm)	100	70 || 100	70 || 100	70 || 100	100	100
Gate Write	E-beam	E-beam	E-beam	E-beam	E-beam	E-beam
Ft (GHz)	60	100	150	300	110	170
Fmax (GHz)	110	180	250	450	160	250
Vbgd (V)	8	12	8	4	40	25
Vds max (V)	7	10	6	3	25	20
Idss (mA/mm)	250(on)/140(off)	500	300	200	700	800
Idss max (mA/mm)	400(on)/180(off)	700	500	400	1100	1200
MIM Capacitors (pF/mm²)	49 & 400	400	400	400	400	400
NF (dB)	0.8 (18 GHz)	1.1 (GHz)	0.8 (30 GHz)	0.5 (30 GHz)	1.5 (40 GHz)	1 (50 GHz)
Power Density (mW/mm)	330	640	300	NA	3300	2000
gm (mS/mm)	450	650	700	1600	650	700

- Higher VDS and IDSS -> Higher power density than GaAs for similar frequency of operation
- Also more power to dissipateÛ

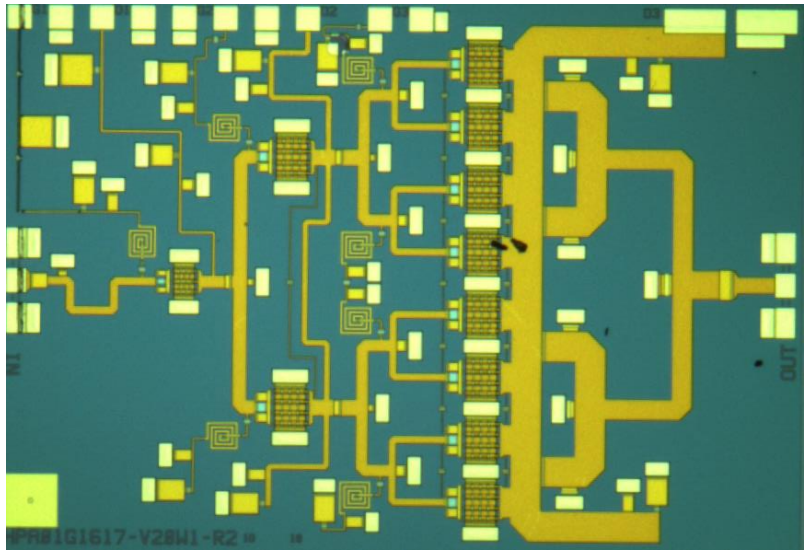
OMMIC GaN on Si Process D01GH

- D01GH
  - 100nm gate length
  - Ft/Fmax = 110/160GHz
  - 3300mW/mm power density
- D006GH
  - 60nm gate length
  - Ft/Fmax = 170/250GHz
  - 2000mW/mm power density

MC2 technologies

20W Ku-Band HPA Example
-
Process D01GH

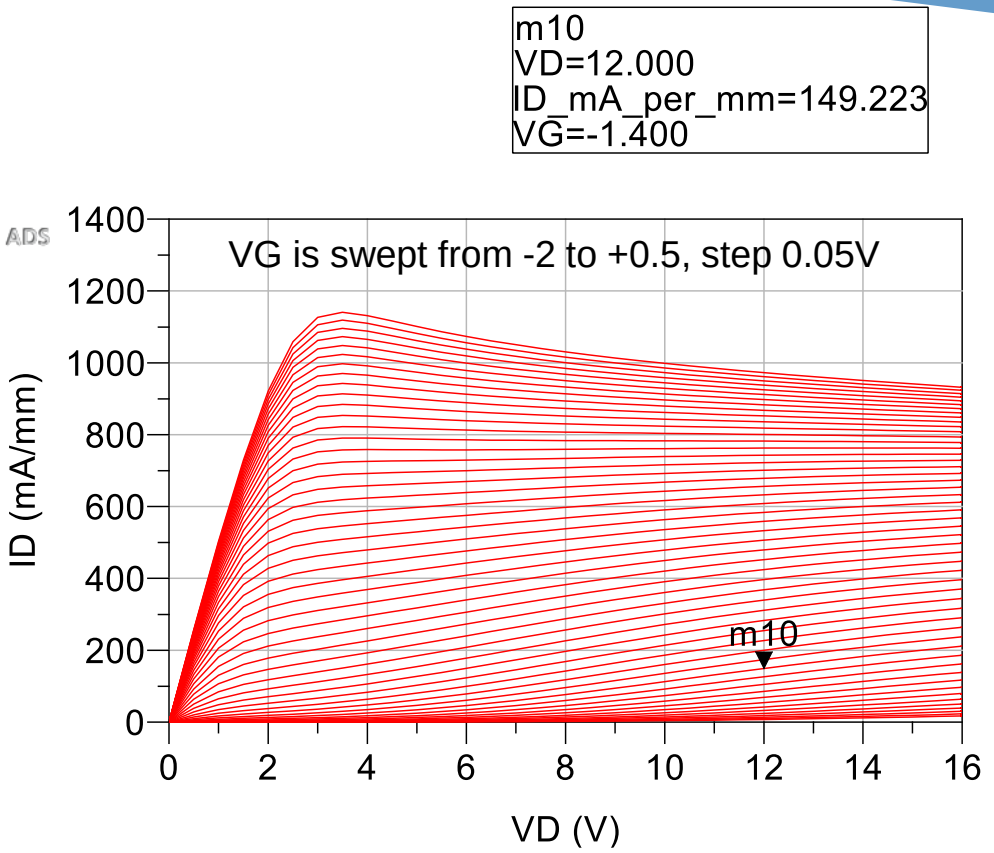
- Bias point and transistor performances
- PA topology
- Zoom on output combining
- Stability
- Measurement results

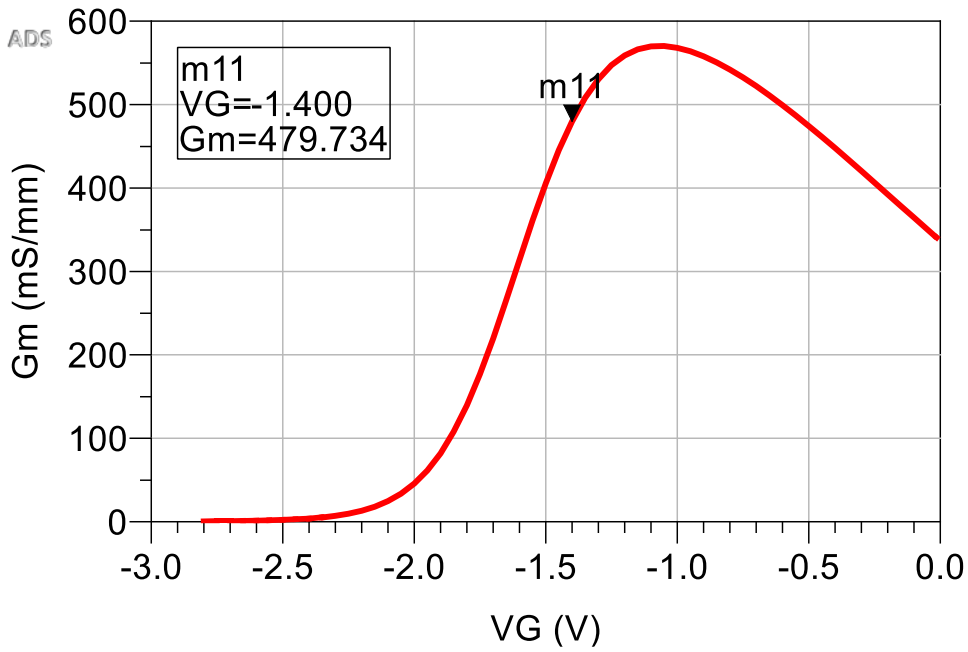


Targeted Ku-Band PA performances

- Freq= 15-18GHz
- Psat ≥ 43dBm (20W) for 4x2.8mm² PA
- PAE ≥ 30%
- Power Gain ≥ 20dB

Ku-Band PA – Transistor bias voltage

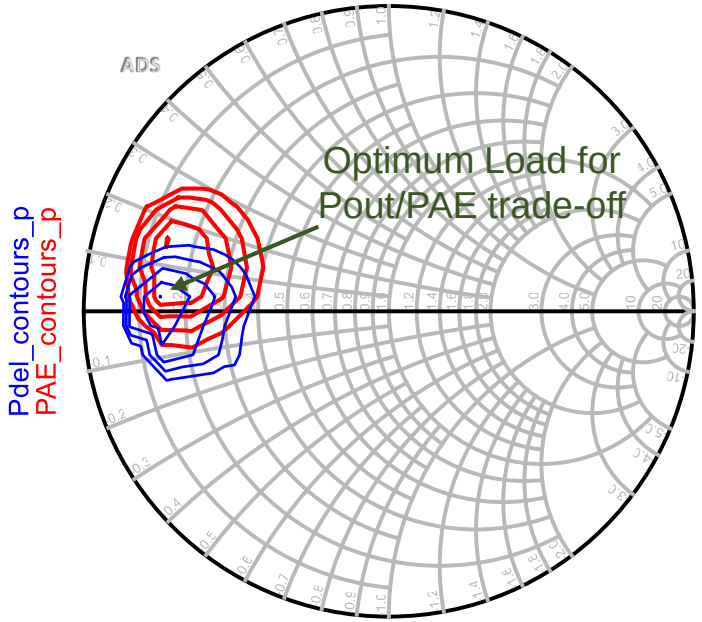




- Drain bias voltage is VD = 12V (recommended)
- Gate bias voltage is VG = -1.4V,
- AB class, usual trade-off between gain and efficiency

Ku-Band PA – Transistor performances

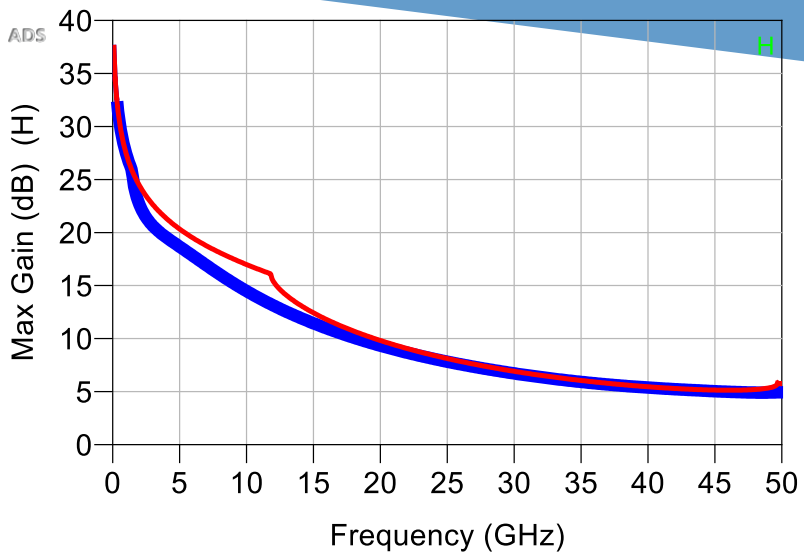
Load-Pull simulation @4dB compression, 8x150um



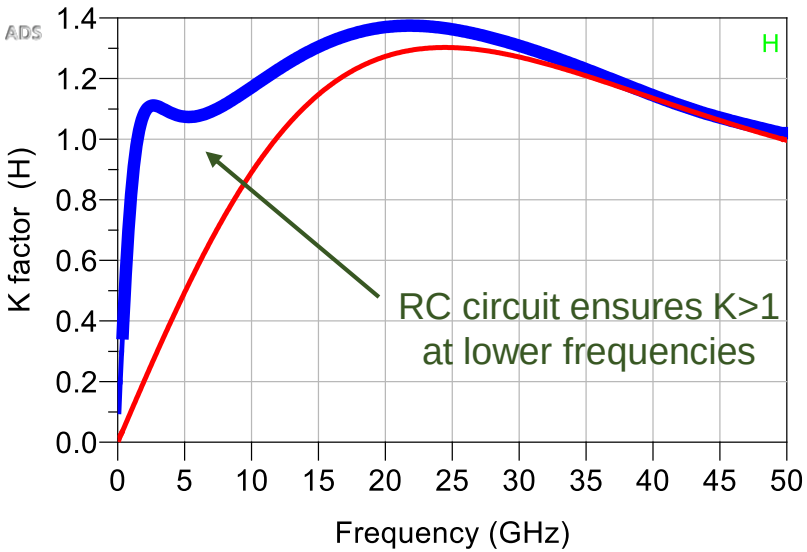
- F=16GHz
- Pout step=0.5dB
- PAE step=4%

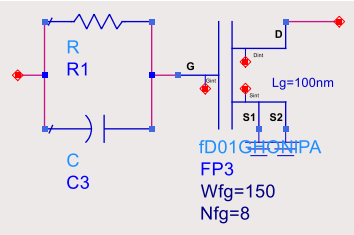
Maximum Power-Added Efficiency, %	Maximum Power Delivered, dBm
54.75	37.45

36.5dBm (single transistor Pout after trade-off) +9dB (combining per 8) -1dB (combining losses) -> Pout > 44dBm is expected



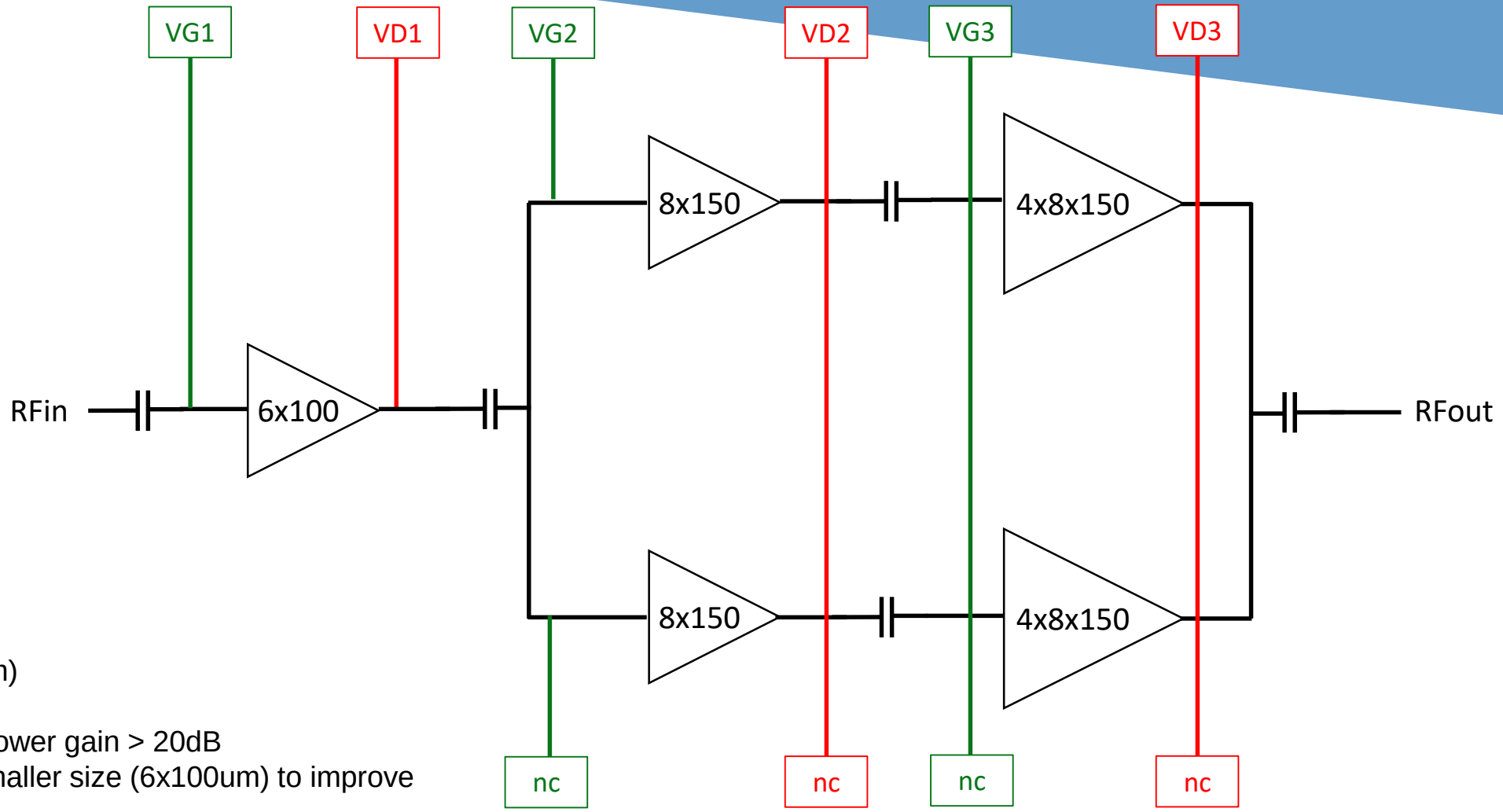
- 8x150um transistor alone
- 8x150um transistor with gate RC circuit
- Max gain is 10dB





This project has received funding from the Clean Sky 2 Joint Undertaking under the European Union's Horizon 2020 research and innovation programme under grant agreement No 821270

Ku-Band PA - Topology

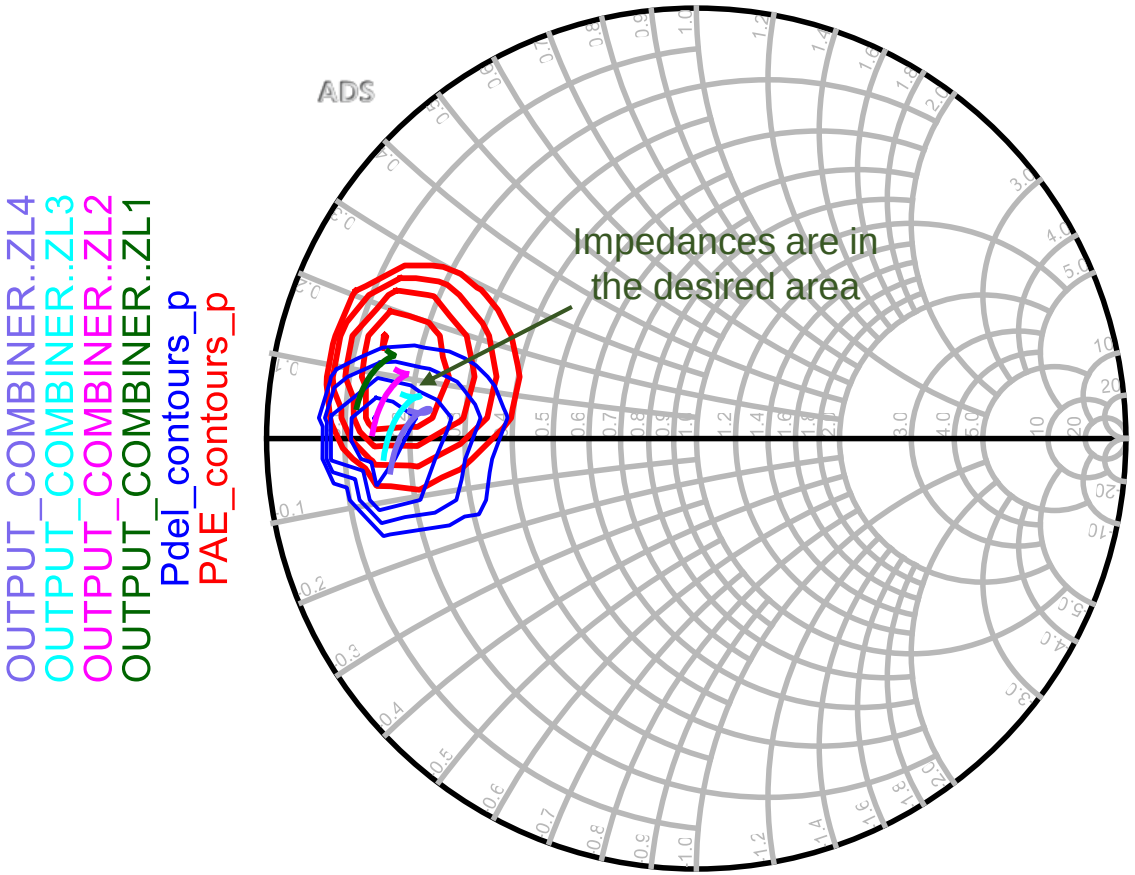


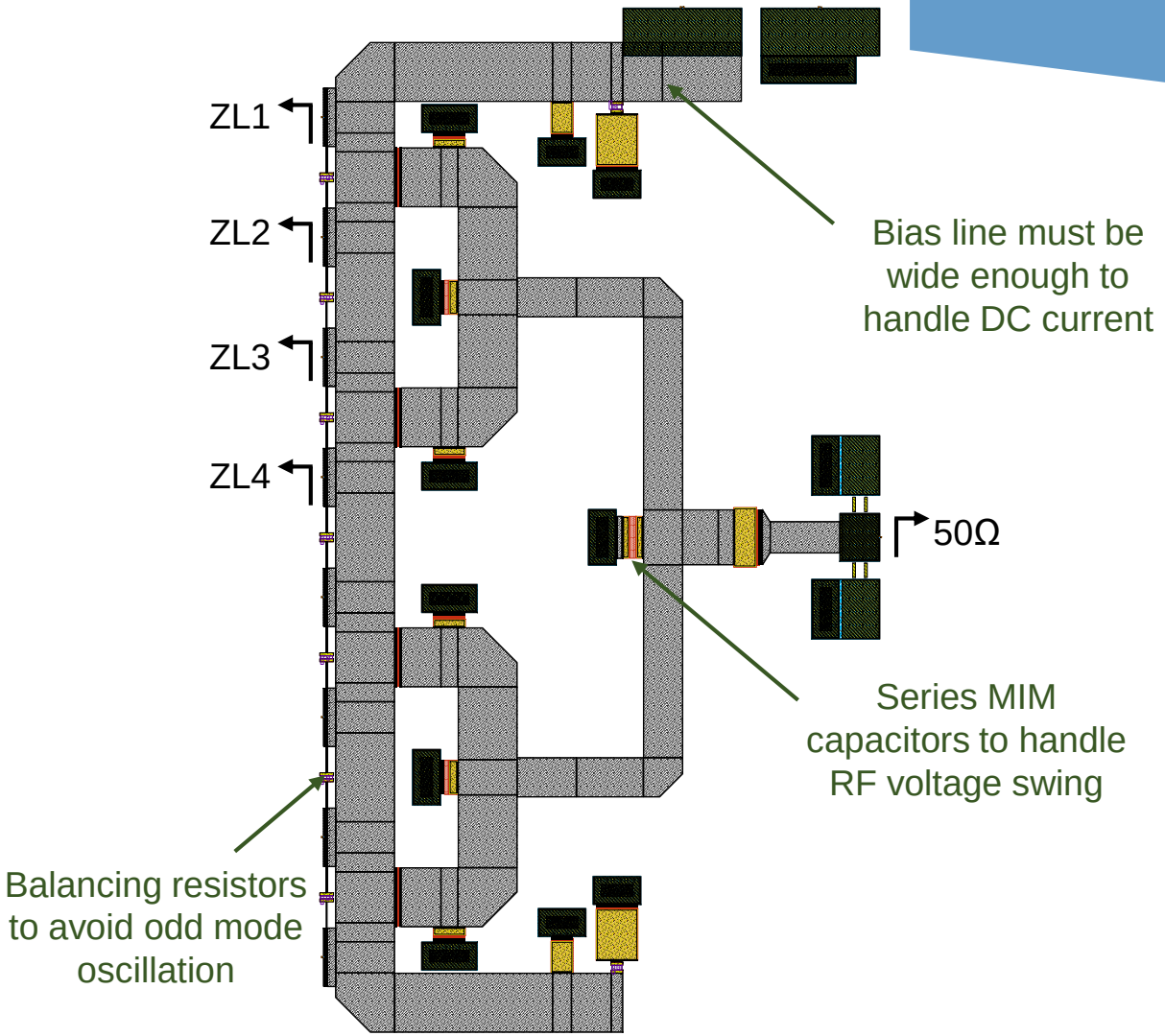
- VD=12 V
- VG=-1.4V (150mA/mm)

- 3 stages needed for power gain > 20dB
- Input transistor has smaller size (6x100um) to improve gain

Ku-Band PA – Power Combiner Zoom

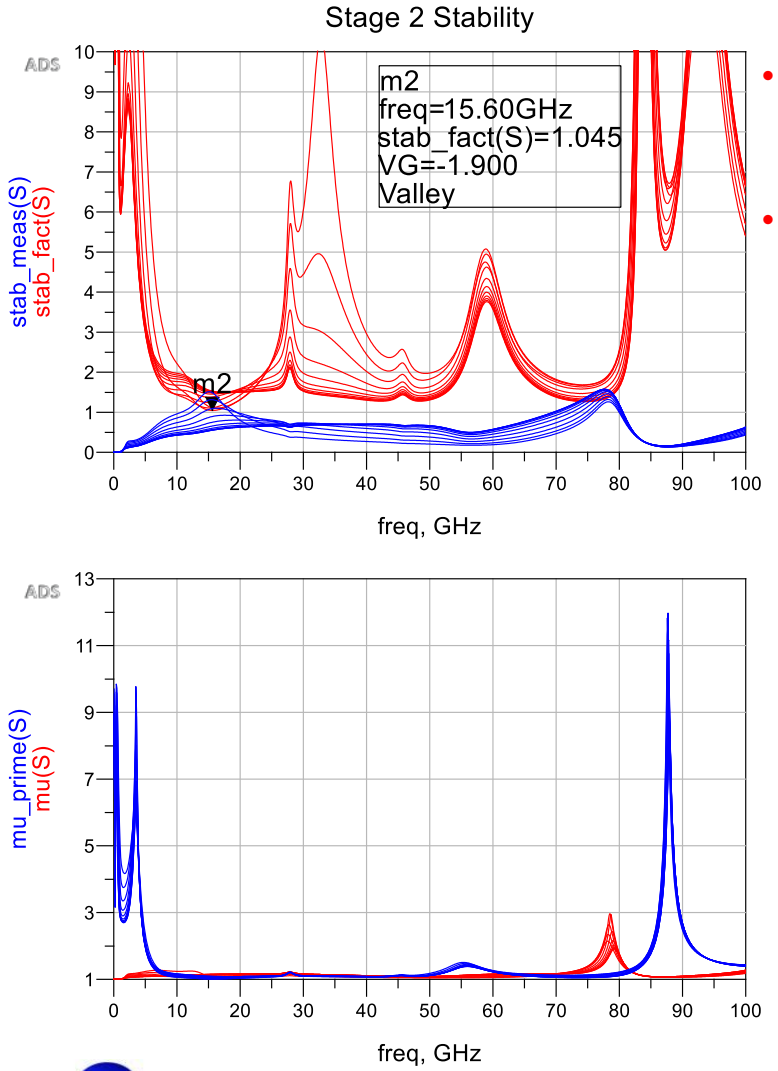
Load-Pull simulation @4dB compression, 8x150um and actual load impedances of output transistors





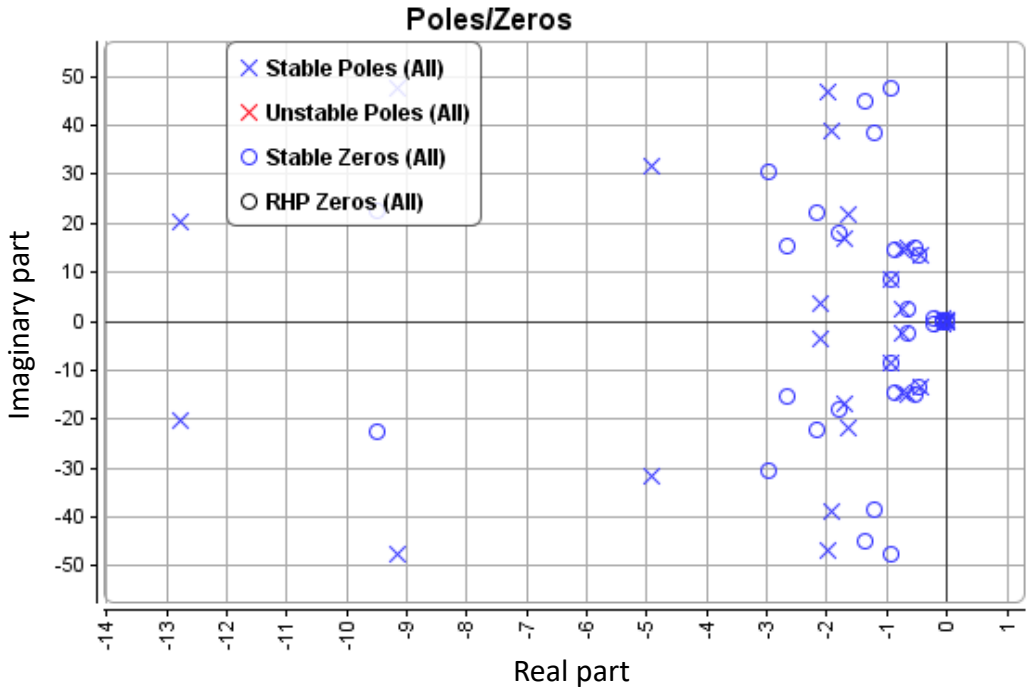
Ku-Band PA – Stability

Example K analysis for PA stage 2, VG sweep



- Small signal analysis
- K should be >1 for unconditional stability

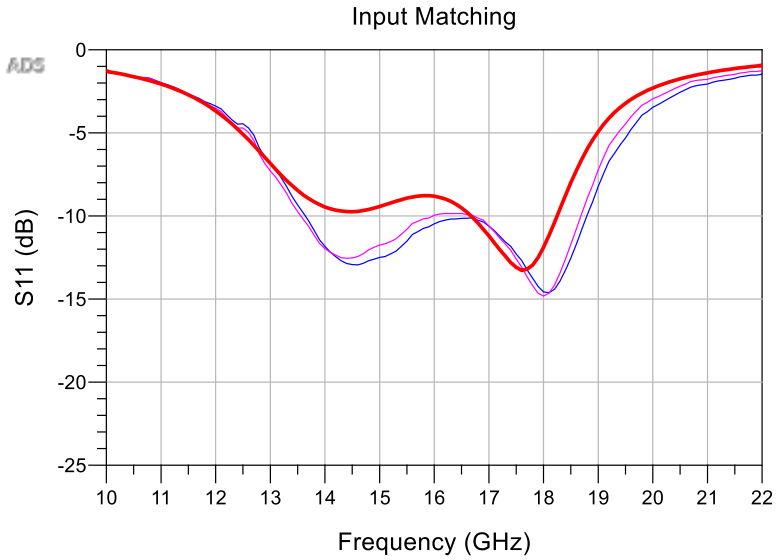
Example Poles/Zeros analysis for PA

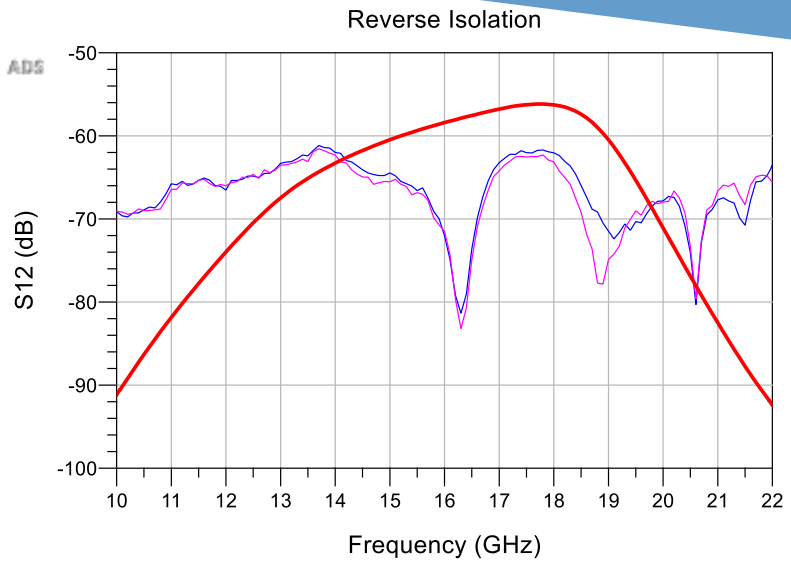


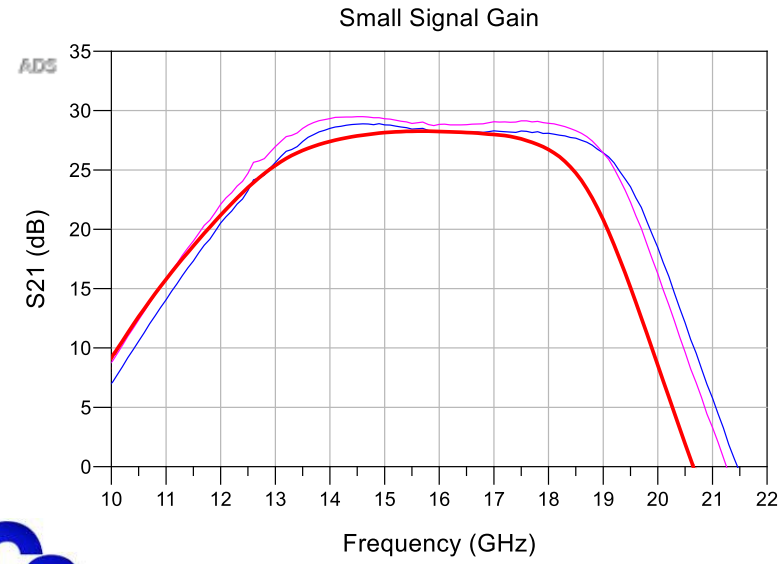
- Poles with positive real part mean unstability
- Oscilation frequency is given by imaginary part
- Input power can be swept (large signal analysis)

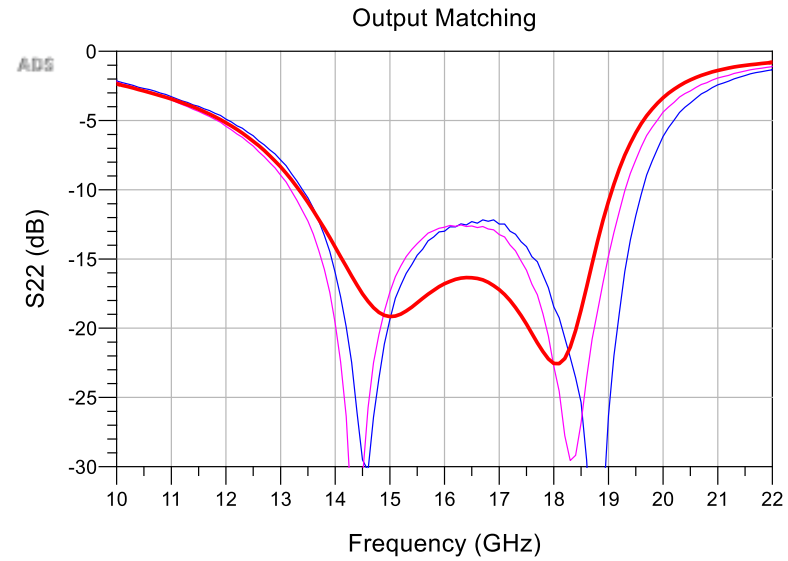
- Stability analysis is mandatory for amplifiers, up to Ft
- Different analysis are recommended: Rollet factor (K factor) for each stage, Transient, Pole/Zero analysis…

Ku-Band PA – S-Parameters Measurements









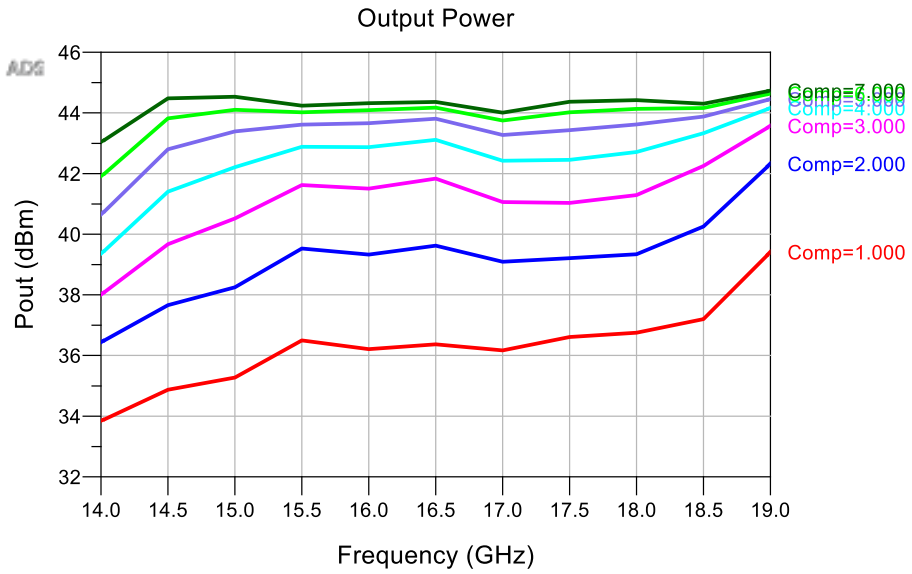
- VD=12 V
- ID0=1950 mA
- CW stage 1
- Pulsed stages 2&3 (5%, 100us)

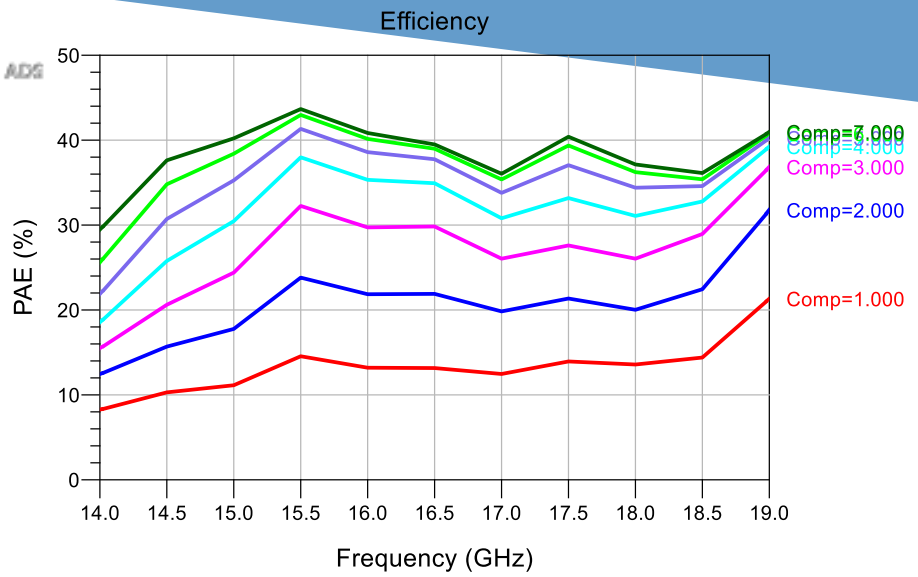
- Simulation
- MMIC 1
- MMIC 2

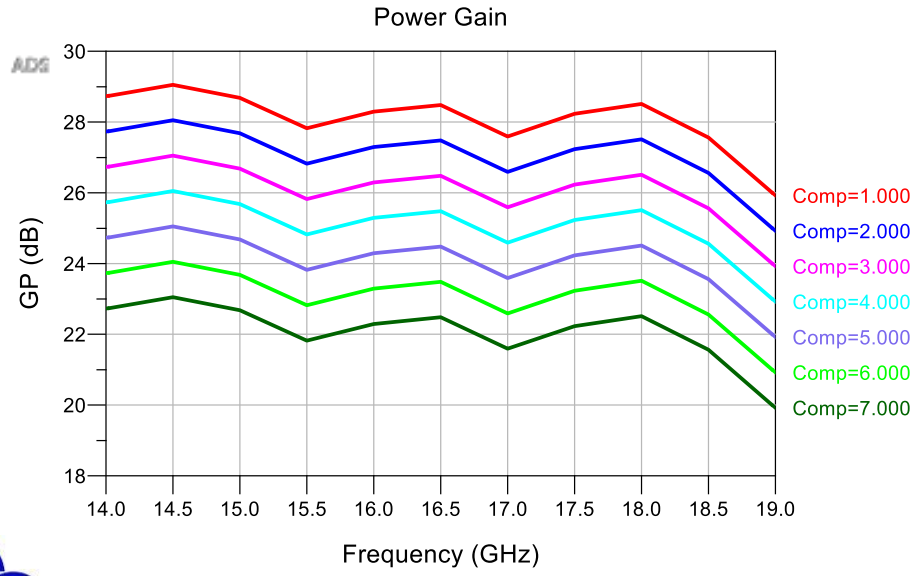
- Matching is better than -10dB in 14-18GHz band
- Small signal gain is 28dB

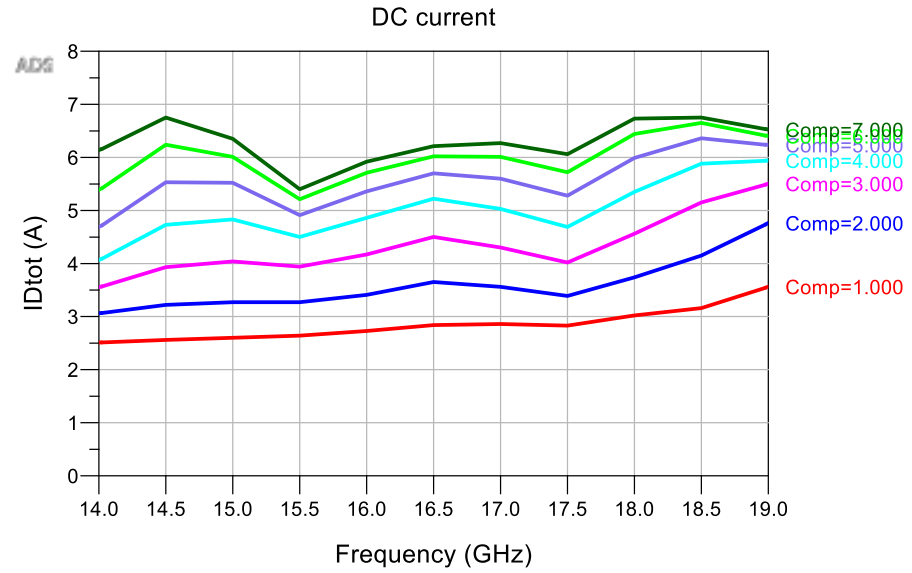
- Slight shift versus simulation

Ku-Band PA – Power Measurements









- VD=12 V
- VG=-1.4 V

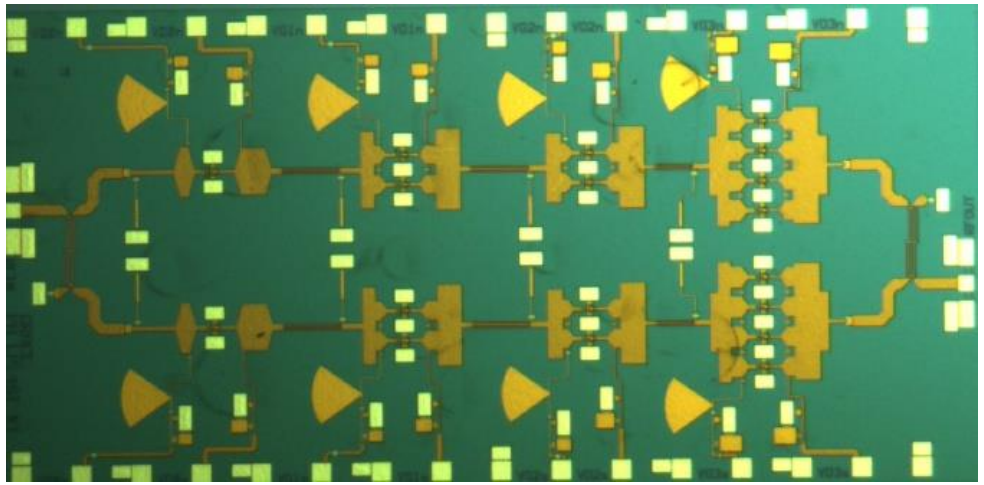
- CW stage 1
- Pulsed stages 2&3 (0.5%, 20us)

- Measured output power is 44dBm with PAE > 35% and GP > 20dB

- High level of compression needed to reach Psat

0.5W W-Band PA Example
-
Process D006GH

- Bias point and transistor choice
- PA topology
- Lange couplers
- Measurement results

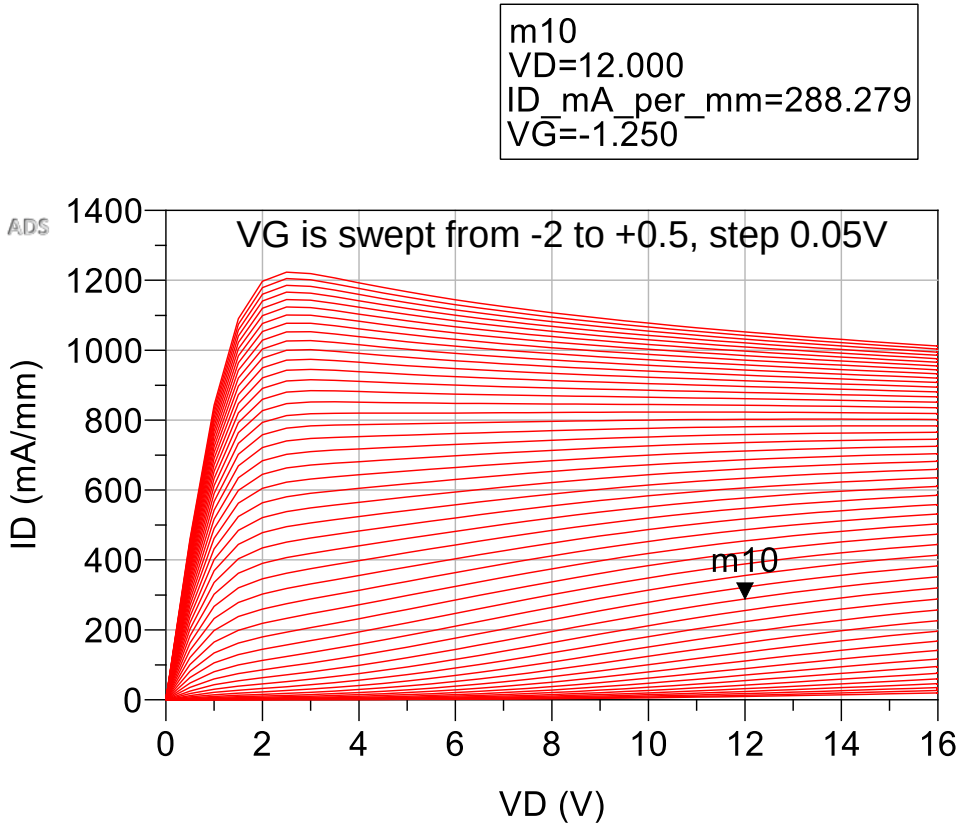


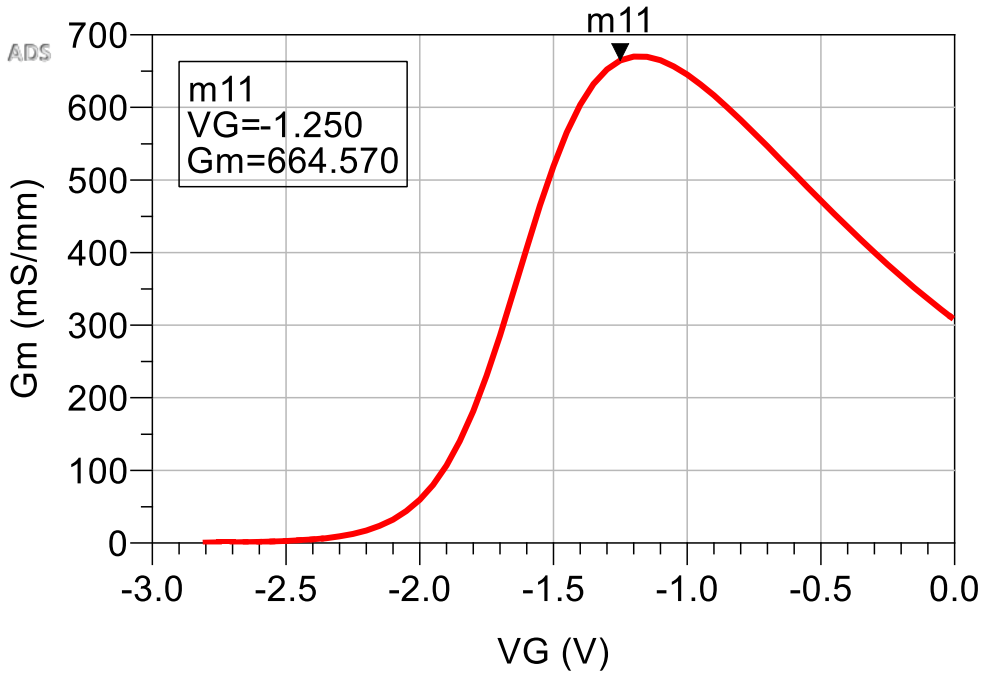
<u>Targeted W-Band PA performances</u>

- Freq= 93-100GHz
- Psat ≥ 27dBm (0.5W)
- Power Gain ≥ 10dB

This project has received funding from the Clean Sky 2 Joint Undertaking under the European Union's Horizon 2020 research and innovation programme under grant agreement No 821270

W-Band PA – Transistor bias voltage choice





- Drain bias voltage is 12V
- Gate bias voltage is near maximum gm for highest gain
- ID is below 300 mA/mm to keep disspiated power below maximum recommended value (3.5 W/mm)

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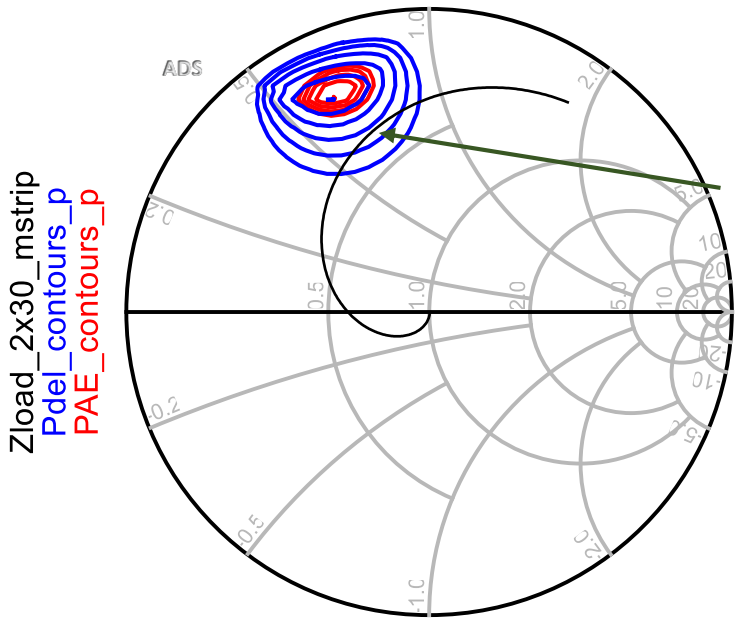
W-Band PA – Transistor performances

Load-Pull simulation @2dB compression, 2x30um

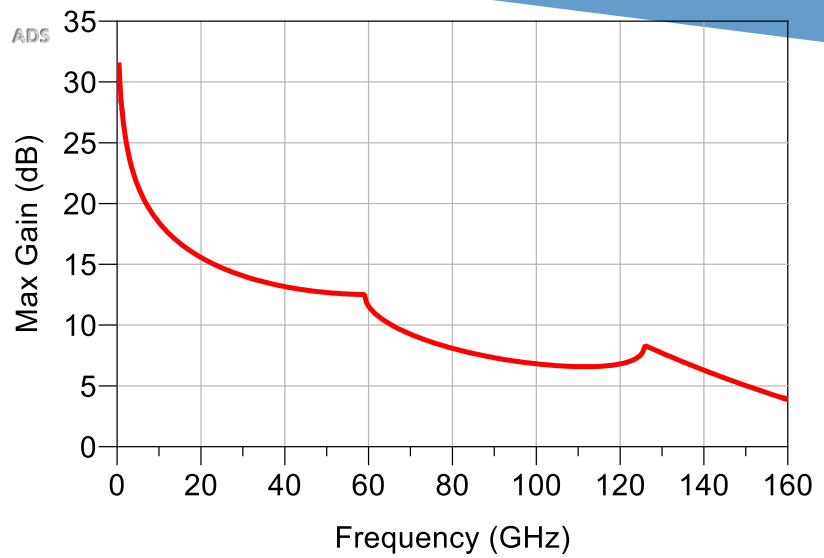


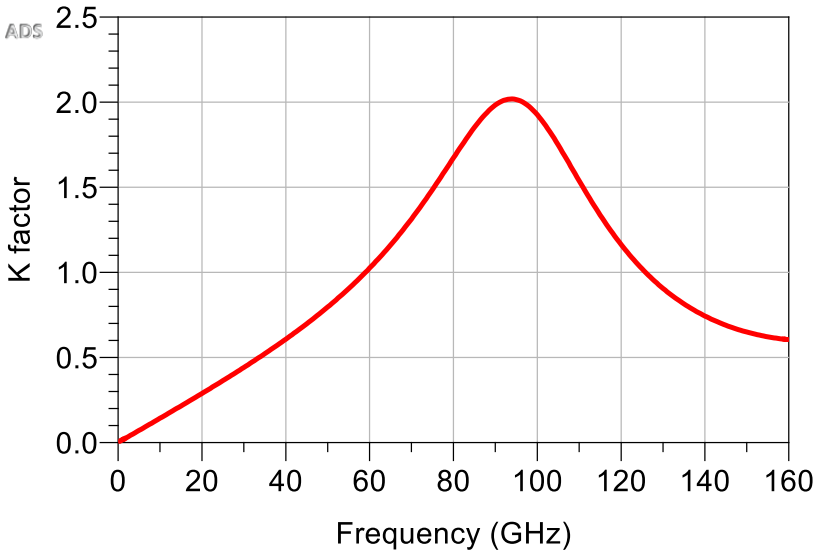
Load impedance is far from optimum

indep(PAE_contours_p) (0.000 to 34.000)
indep(Pdel_contours_p) (0.000 to 84.000)
freq (500.0MHz to 150.0GHz)

- F=97GHz
- Pout step=1dB
- PAE step=2%
- Gain step=0.5dB

Maximum Power-Added Efficiency, %	Maximum Power Delivered, dBm
37.10	23.58





- 2x30um transistor alone
- Max gain is 6.5dB at 100GHz
- Stability is unconditional from 60 to 130GHz

- Optimum impedance area is close to the edge of the Smith chart and very selective -> Maximum delivered power per transistor will be around 20dBm -> 8 transistors are needed to reach Pout > 27dBm

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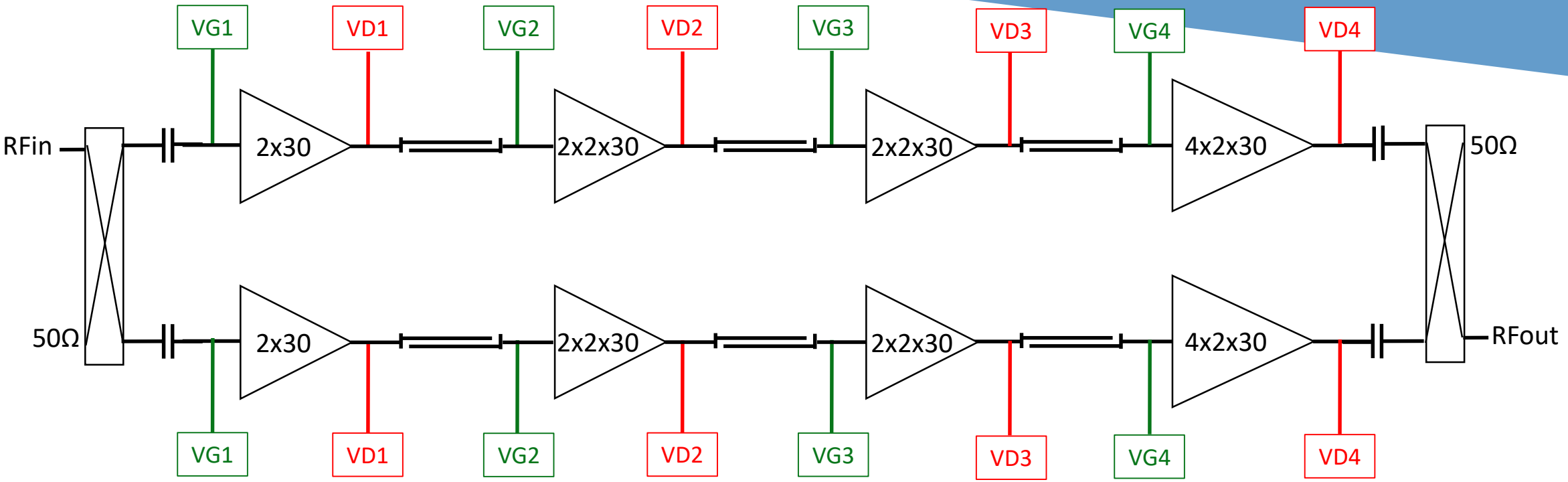
W-Band PA - Topology



- VD=12 V
- VG=-1.25V (300mA/mm)

- 4 stages needed for usable power gain
- Lange couplers used for good input/output matching and isolation between north and south amplifier branches

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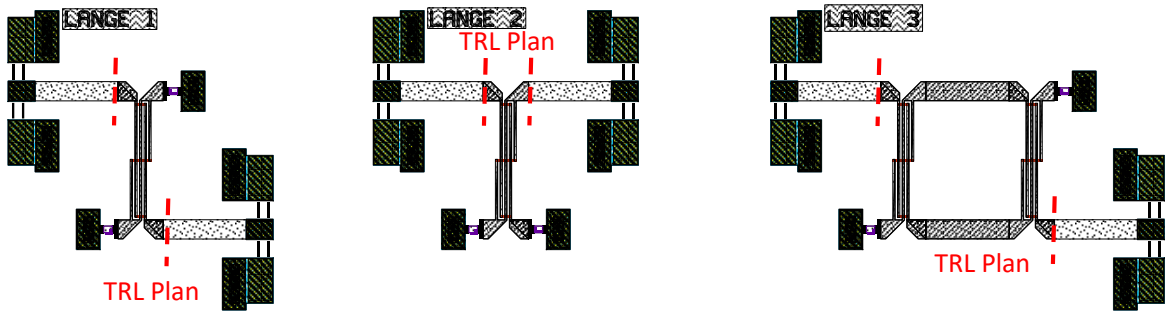
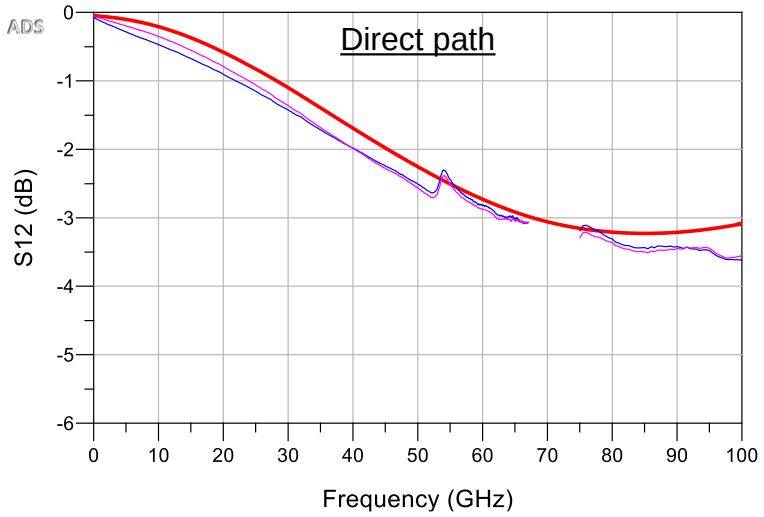
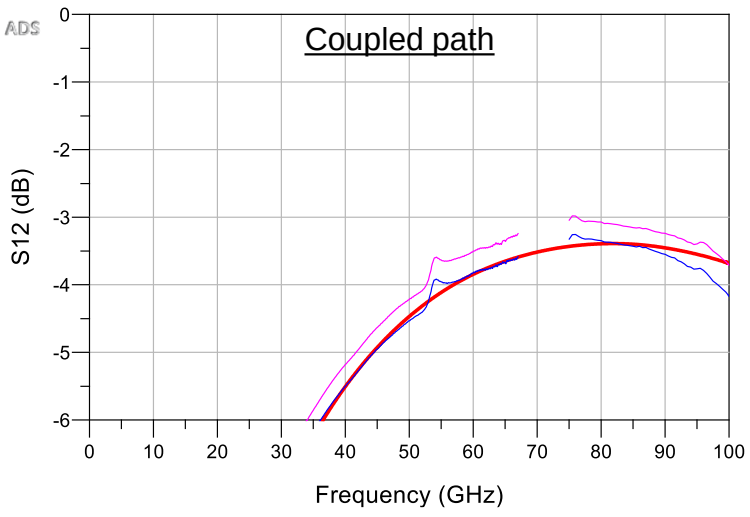
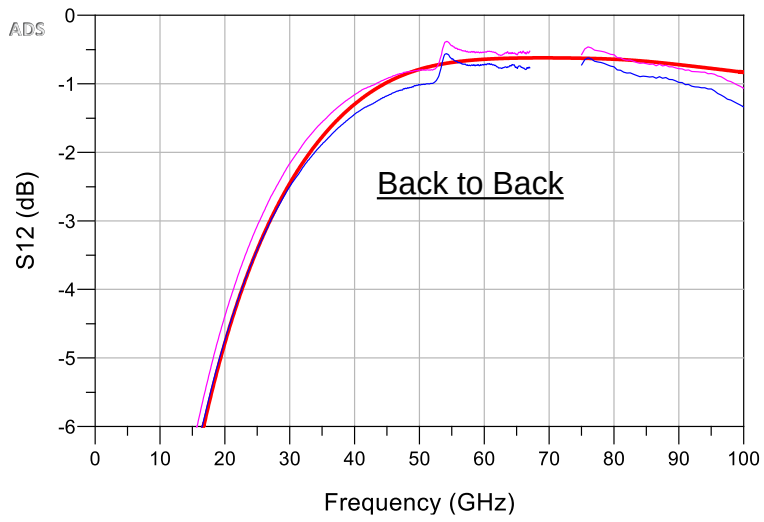
W-Band PA – Lange Power Combiner



- TRL calibration
- EM Simulation
- Measurement (Ret 1805)
- Measurement (Ret 1813)







- TRL calibration to remove GSG pad impact on measurement
- Measured (TRL) Back to Back Lange couplers losses are around 1dB
- In line with simulation

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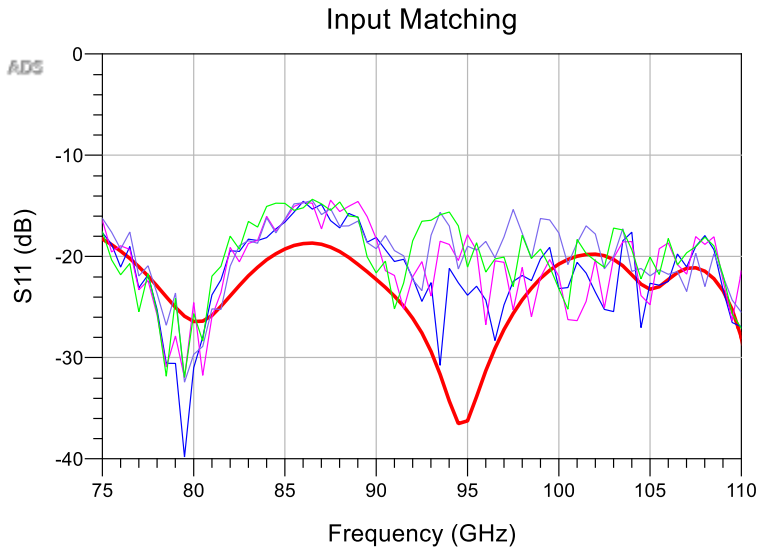
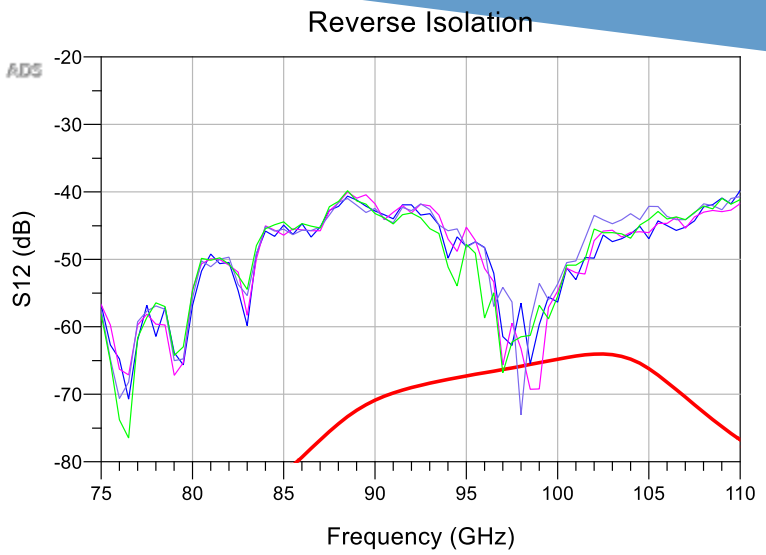
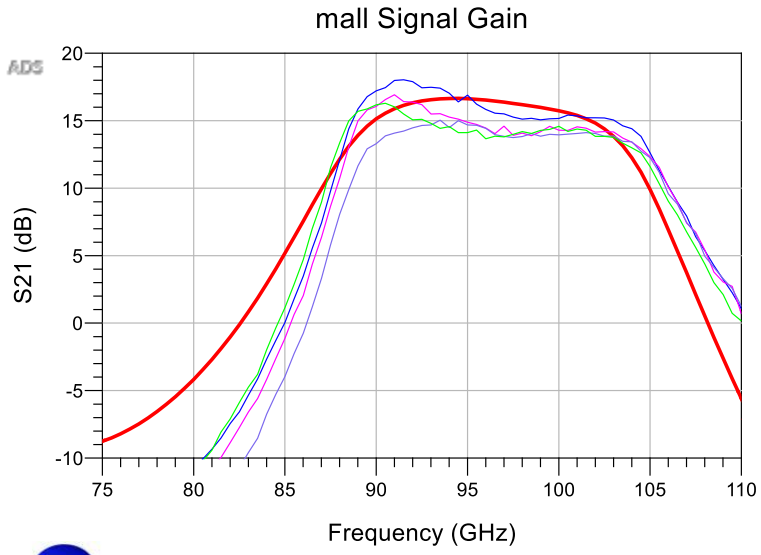
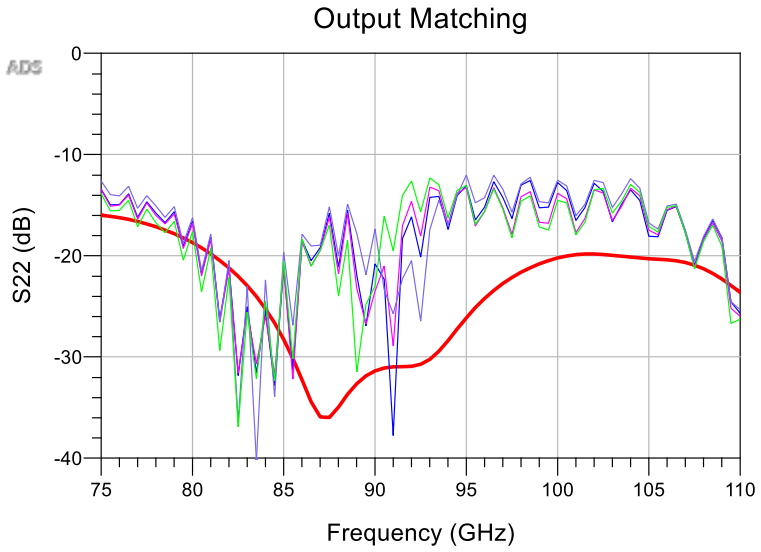
W-Band PA – S-Parameters Measurements









- VD=12V,
- Nominal bias: 300mA/mm, 3.6W/mm
- Total dissipated power in pulse is 3.9W

- Stage 0&1 are CW
- Stage 2&3 are pulsed (50us, 5%)

- Simulation
- MMIC 1
- MMIC 2
- MMIC 3
- MMIC 3

- Small signal gain is around 15dB
- Input and Output Matching are better than -10dB

- Mostly In line with simulation

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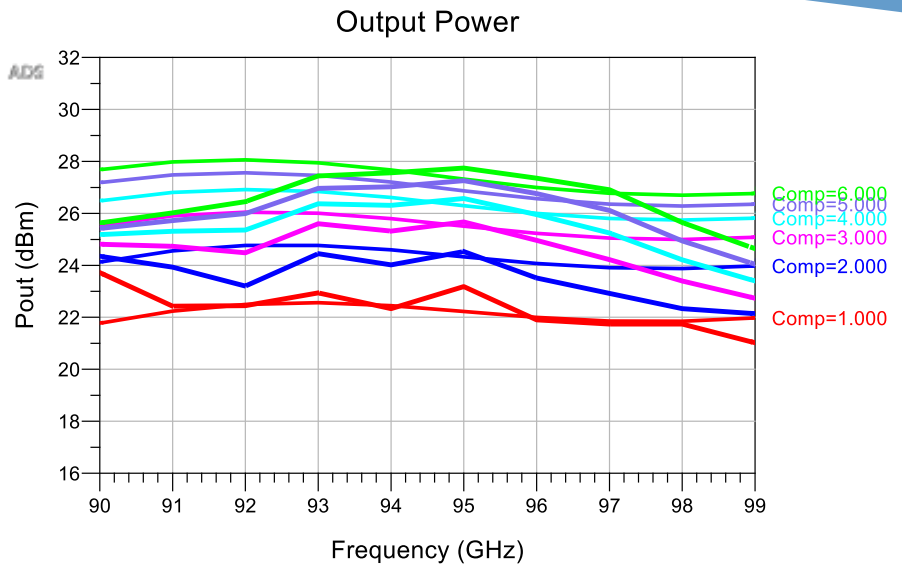
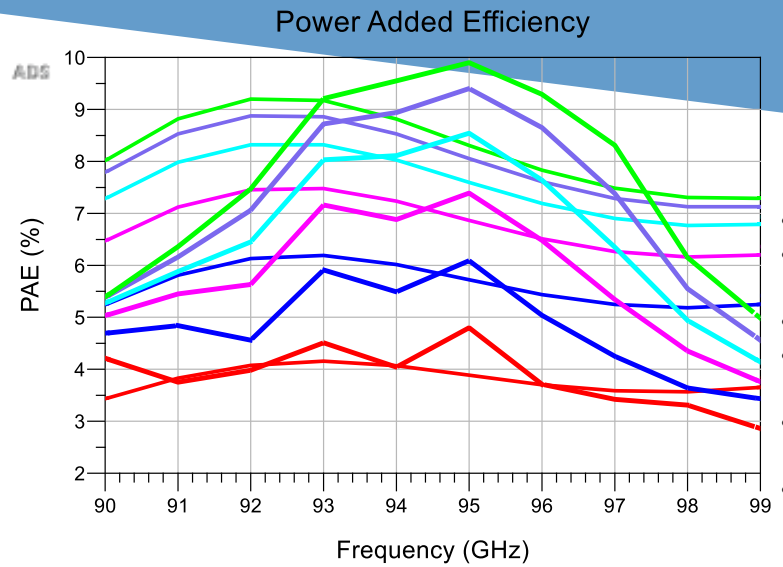
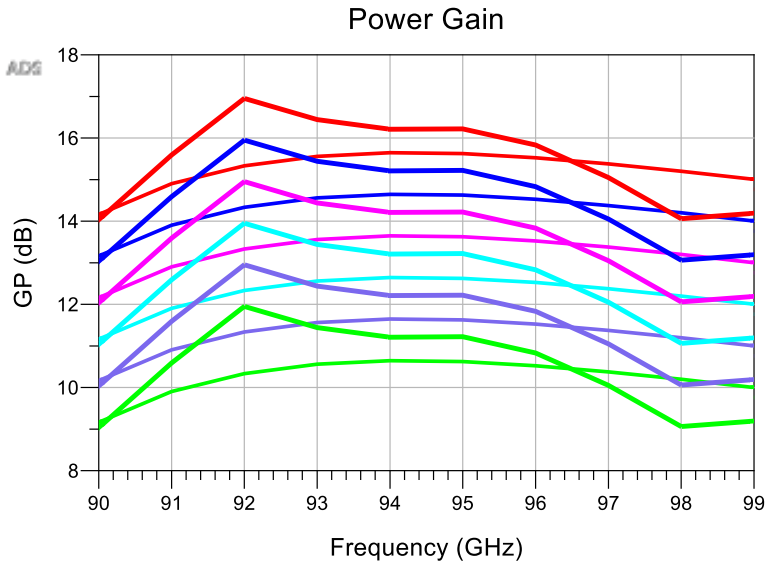
W-Band PA - Power Measurements





- VD=12V,
- Nominal bias: 300mA/mm, 3.6W/mm
- Stage 1&2 are CW
- Stage 3&4 are pulsed (50us, 5%)
- Dots: Measurement
- Line: Simulation



- Pout is > 27dBm in 93-97GHz band (P6dB)
- PAE is around 9%
- GP is around 10dB (P6dB)

- Measured output power level is close to expected level, though power performances are a bit narrower than simulation

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Thank you !

contact@mc2-technologies.com www.mc2-technologies.com +33 3 20 04 55 67