EuMW 2019
UNIVERSALITY THROUGH MICROWAVES

EUROPEAN MICROWAVE WEEK 2019
SIX DAYS · THREE CONFERENCES · ONE EXHIBITION
PORTE DE VERSAILLES PARIS, FRANCE
29TH SEPTEMBER - 4TH OCTOBER 2019
Exhibition Hours:
Tuesday, 1st October 9.30 - 18.00
Wednesday 2nd October 9.30 - 17.30
Thursday 3rd October 9.30 - 16.30
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OMMIC
innovating with III-V'S

EuMIC08-1

Ka to W Band GaN/Si Power Amplifiers

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OMMIC
innovating with III-V'S

1st
6 Inch GaN line in Europe

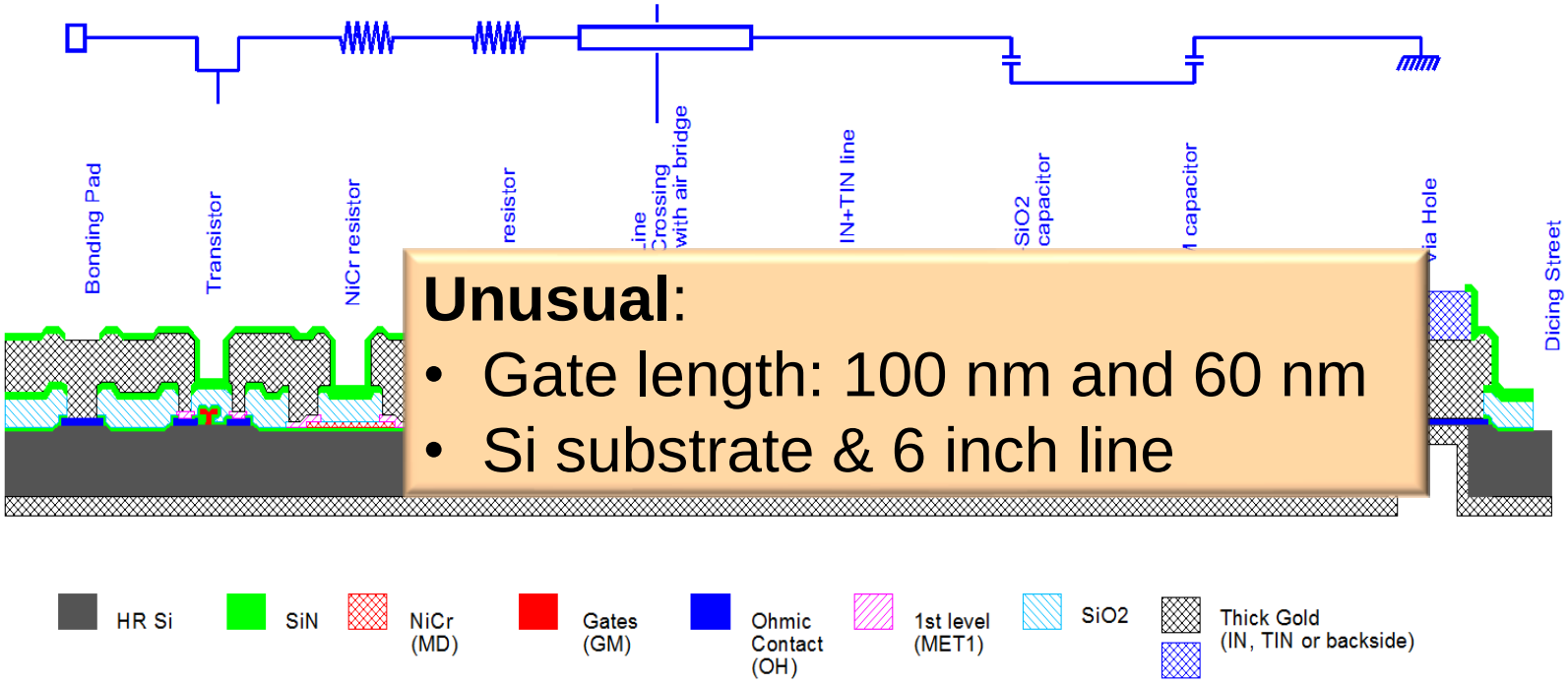
- Created in 2000, III-V activities started in 1970
- Former Philips Semiconductor division
- Over 49 years of experience in III-V semiconductors, including GaAs and InP
- Unique GaN Process best suited for upcoming 5G
- Only foundry in Europe offering complete service including Epitaxial Growth, Process Development, MMIC Design & Fabrication, Test & Product Qualification

To meet us …

20 km

OMMIC GaN/Si MMIC process

Full MMIC Process for mm-wave designs
Via holes, air-bridges, metal resistors, MIM capacitors



Unusual:

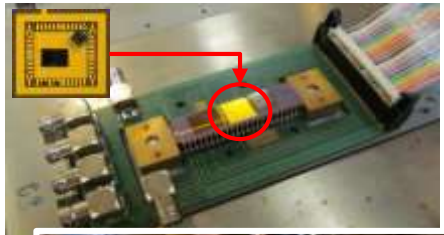
- Gate length: 100 nm and 60 nm
- Si substrate & 6 inch line

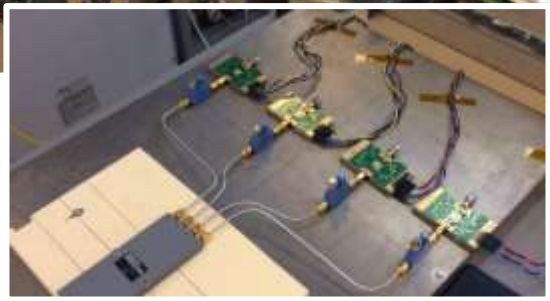
techd01gh.skd

Si substrate !! Why not SiC ??

- Cons…
  - Higher Rth ?
    - Yes, but in fact only x2, compatible with the power levels required at mm wave and with the 12V quiescent voltage of OMMIC GaN
  - Higher microwave losses ?
    - We use HR Si with good buffer, only 0.3dB/mm@30 GHz
- Pros…
  - Lower cost, larger diameters, thus compatible with 5G volumes
  - Lower risk of import/export restrictions
  - Compatible with heterogeneous integration with SiGe/CMOS

OMMIC GaN/Si process reliability





Reliability evaluation completed in the frame of a Thales CS / DGA contract

- **Storage** 3 temperatures
- DC life test at **6 channel temperatures** and 2 VDDs (12V & 15V)
- **HTRB** tests at 2 reverse biasing points (24 & 30V)
- RF step stress up to **7dBc** by steps of 168h
- **RF life test** at 3dBc
- **MTTF 3.10^7 hours** at 200°C channel temperature

Full ESCC-compatible Space Evaluation running in the frame of H2020 MiGaNSOS project, with UTV, TAS-I, VTT, OMMIC

The MIGANSOS project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 779305

OMMIC GaN/Si process from statistics

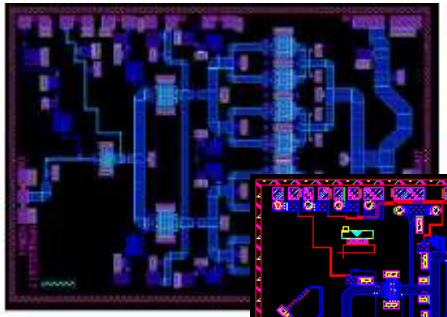
Electrical Characteristic	Gate 100 nm	Gate 60 nm
Frequency Cutoff	105 GHz	130 GHz
MSG at 30 GHz (2x25µm device)	13 dB	13.5 dB
RF power density	3.3 W/mm	3.3 W/mm
NF min at 40 GHz	1.5 dB	1.1 dB
Extrinsic Transconductance	800 mS/mm	950 mS/mm
Extrinsic Drain Source resistance (Ron)	0.6 Ω.mm	0.6 Ω.mm
Gate Drain voltage for 300µA/mm	>50 V	>50 V
Maximum Drain Current at Vds=3V	1.3 A/mm	1.6 A/mm
Recommended Quiescent VDD	12 V	12 V

Tips to design PAs with OMMIC GaN/Si

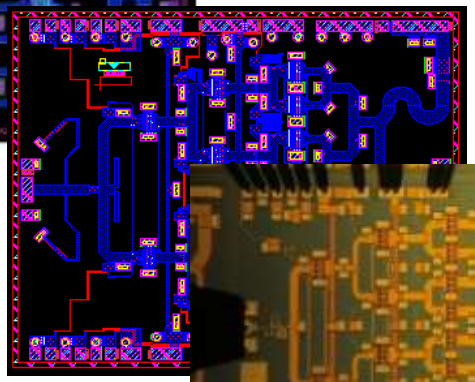
- Gain is high !
  - 800 µm devices can be used even at 40 GHz
  - Use stabilization networks in X or Ku band
- Usual Quiescent voltage is 12 V
  - Breakdown is above 50 V
- Usual biasing is AB class (Imax/8, approx 200 mA/mm)
- Loadlines of individual transistors should be set by design to maintain dissipated power (Pdiss) below 3.5 W/mm (2.5W/mm for space) in large signal (CW)
  - Pdiss = PDC + PRFin – PRFout = PDC × (1 - PAE)

A few examples of PAs

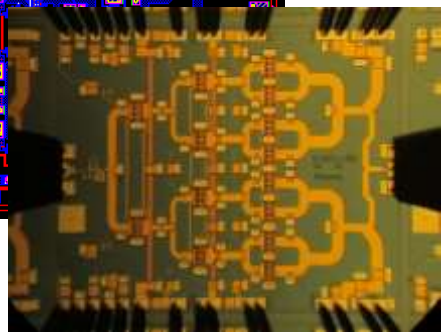
15-18 GHz, 43 dBm



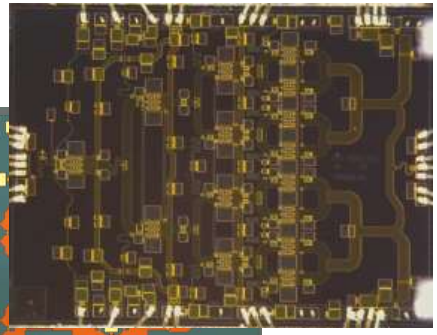
27-31 GHz, 41.5 dBm



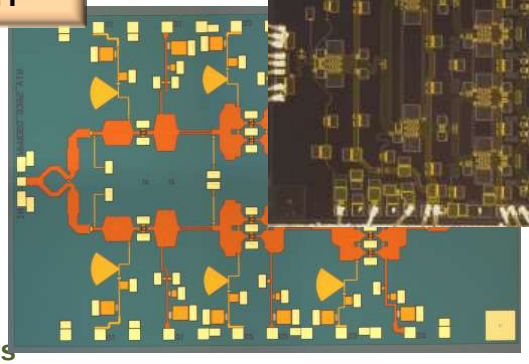
37-43 GHz, 41 dBm



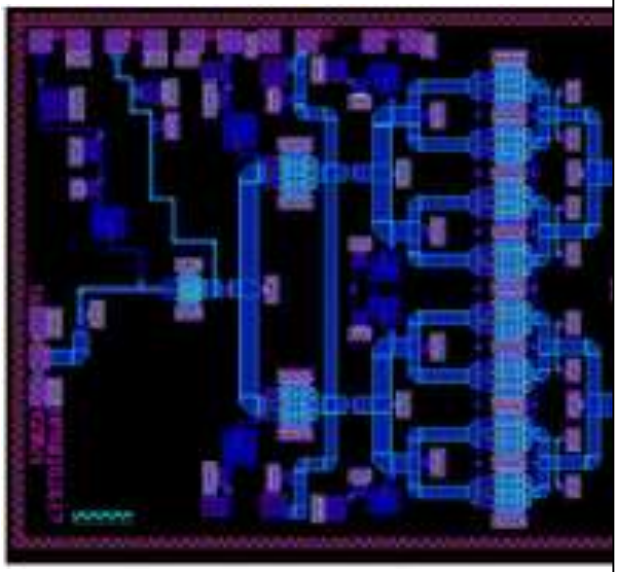
48 GHz, 41 dBm

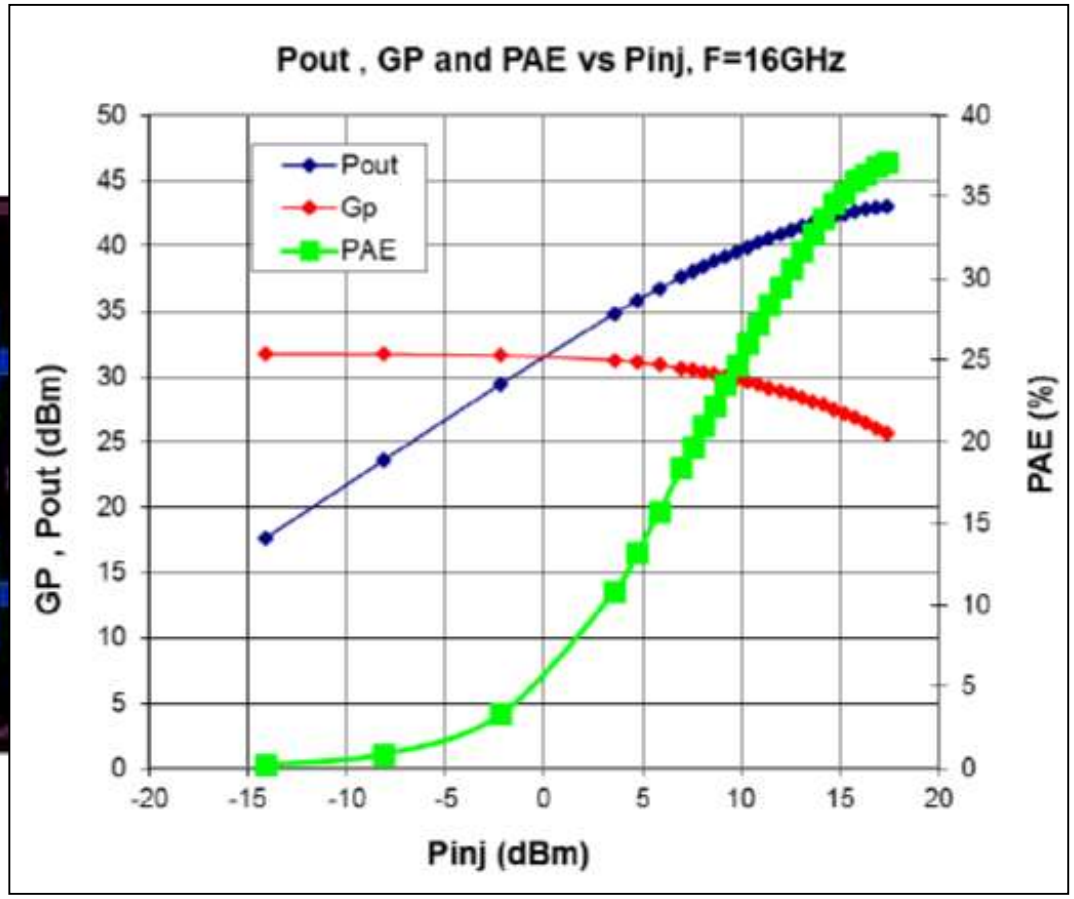


90 GHz, 28 dBm



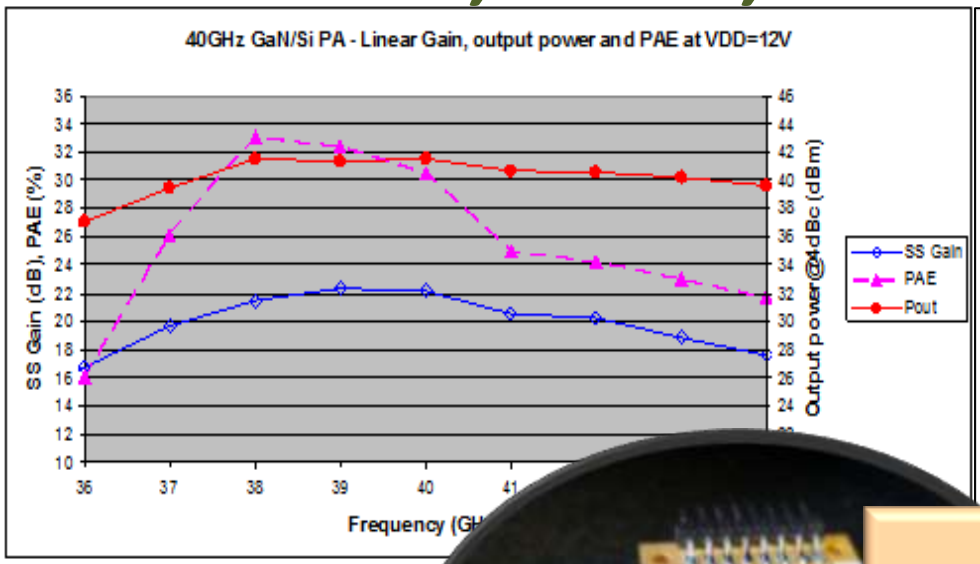
15-18 GHz, 20 W, 37% PAE

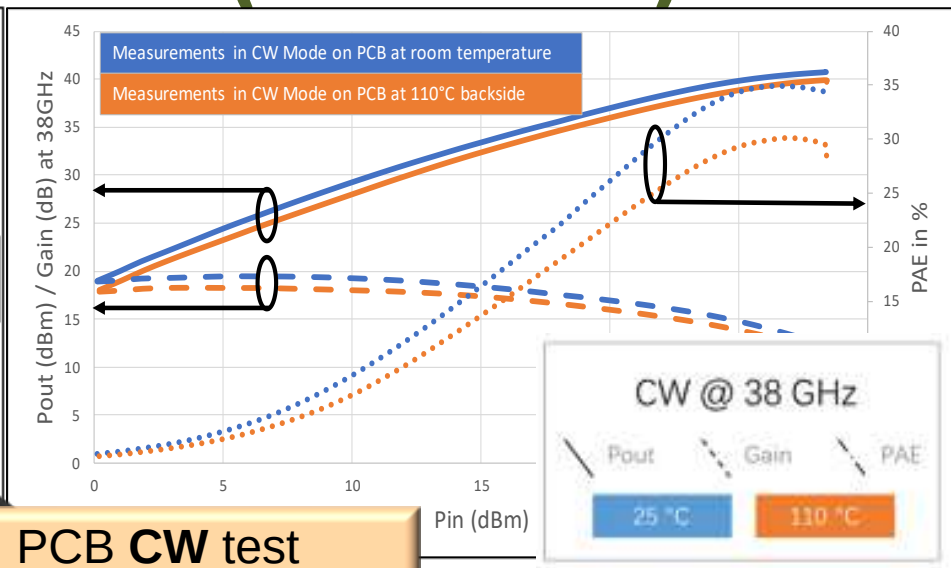




On wafer pulsed test

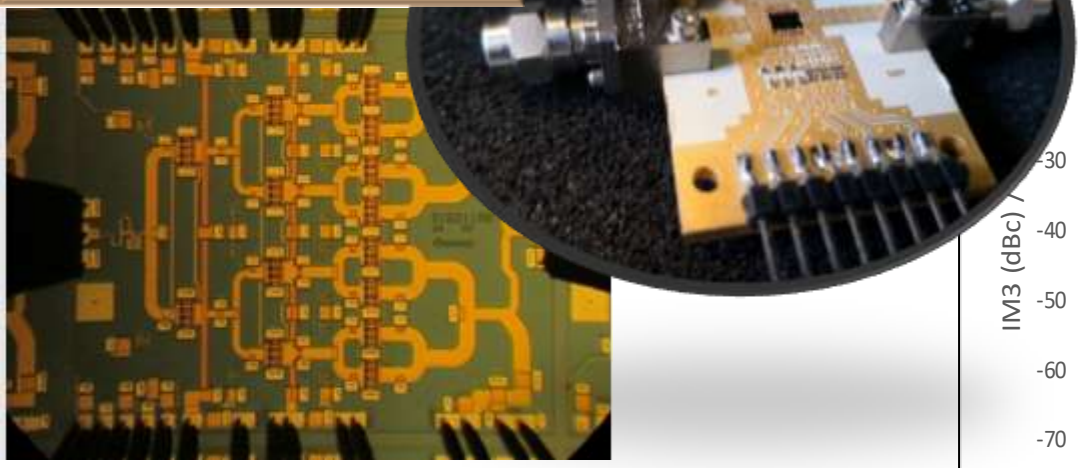
37-43 GHz, 10 W, 30% PAE (CGY2651)

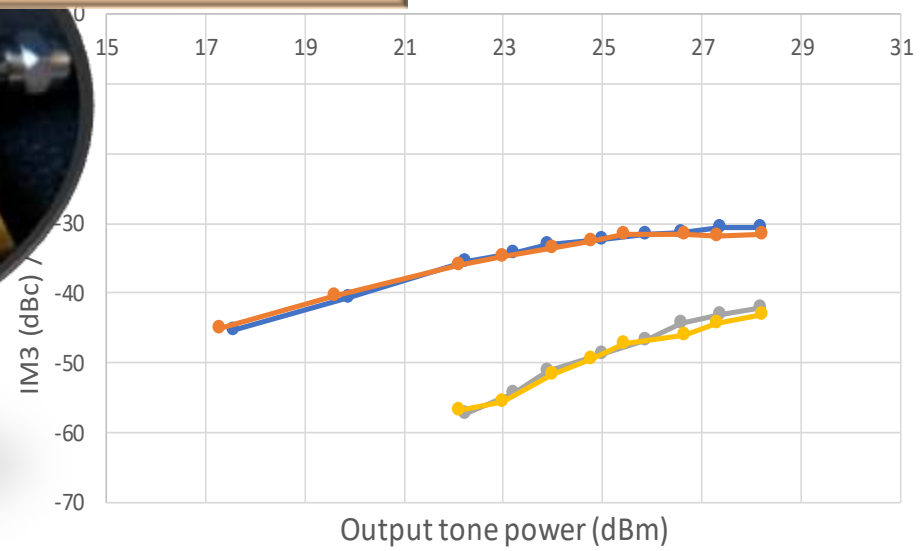




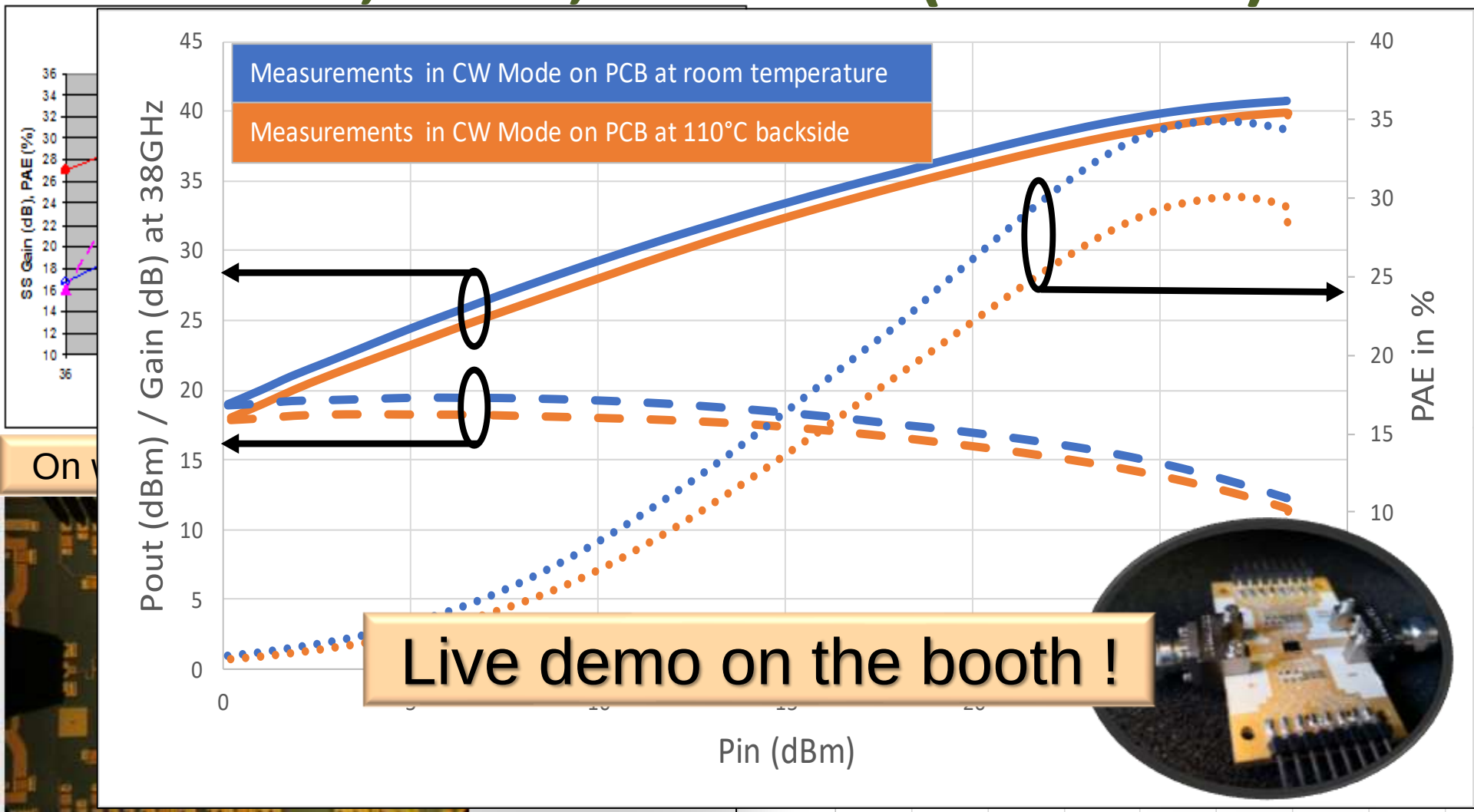
On wafer pulsed test

PCB **CW** test



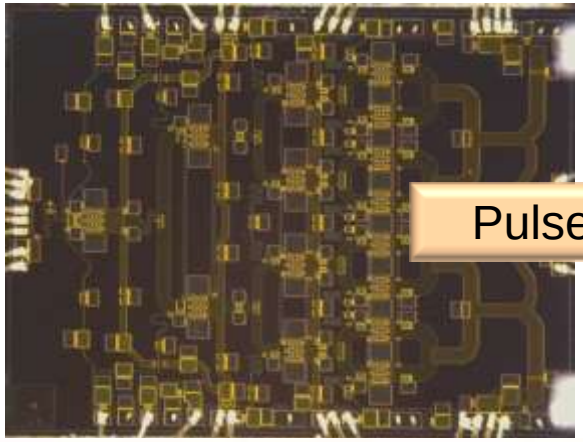


37-43 GHz, 10 W, 30% PAE (CGY2651)

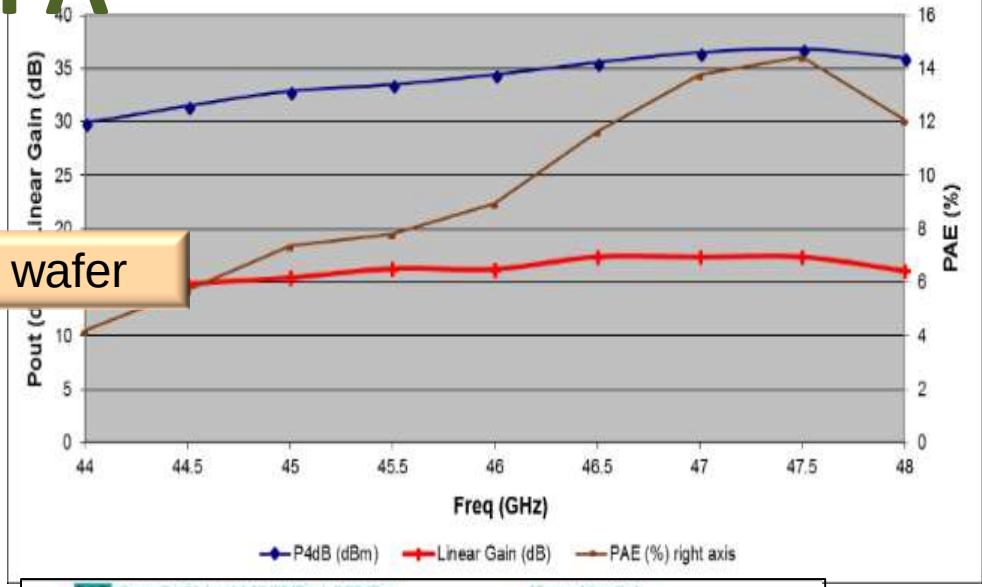


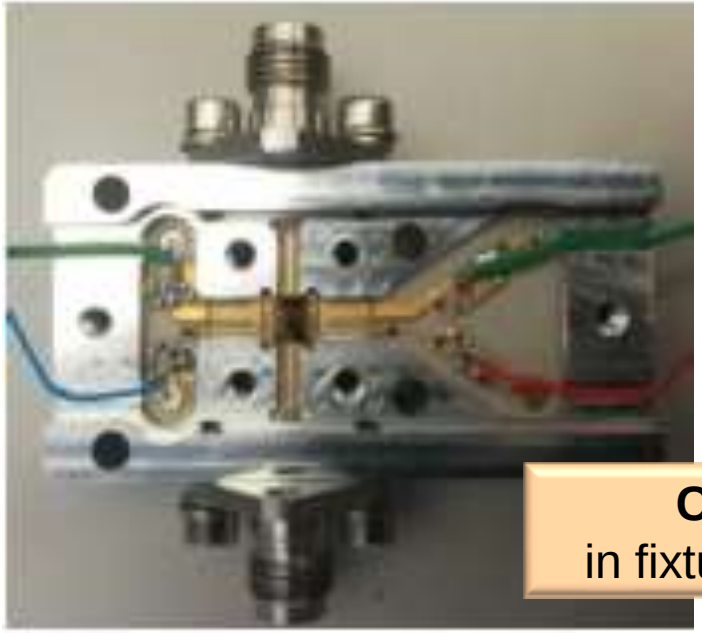
CGY2651 CW live demo at EuMW 2019

48 GHz, 5 W, V band PA

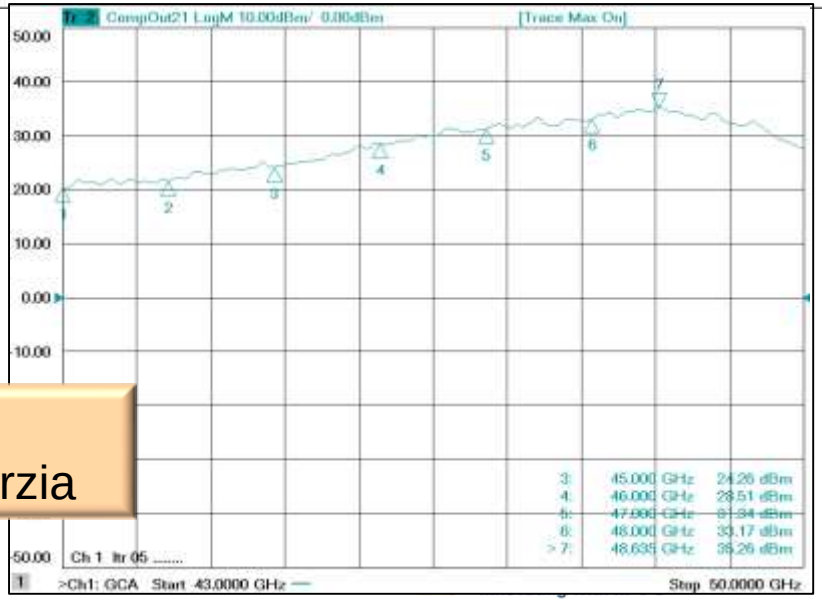


Pulsed test, on wafer

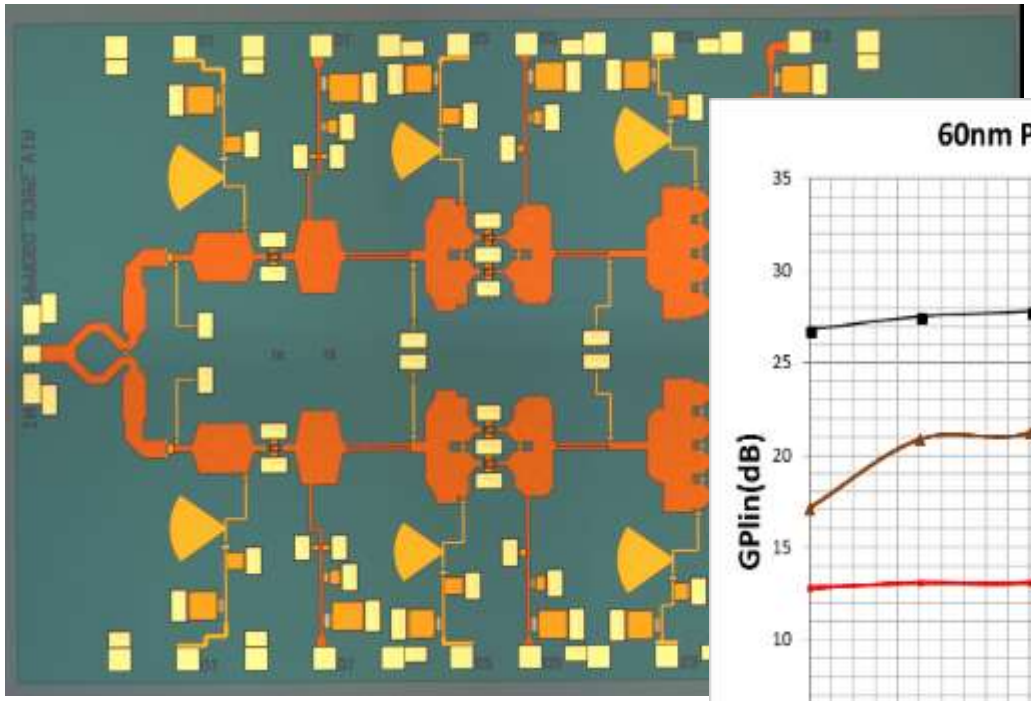




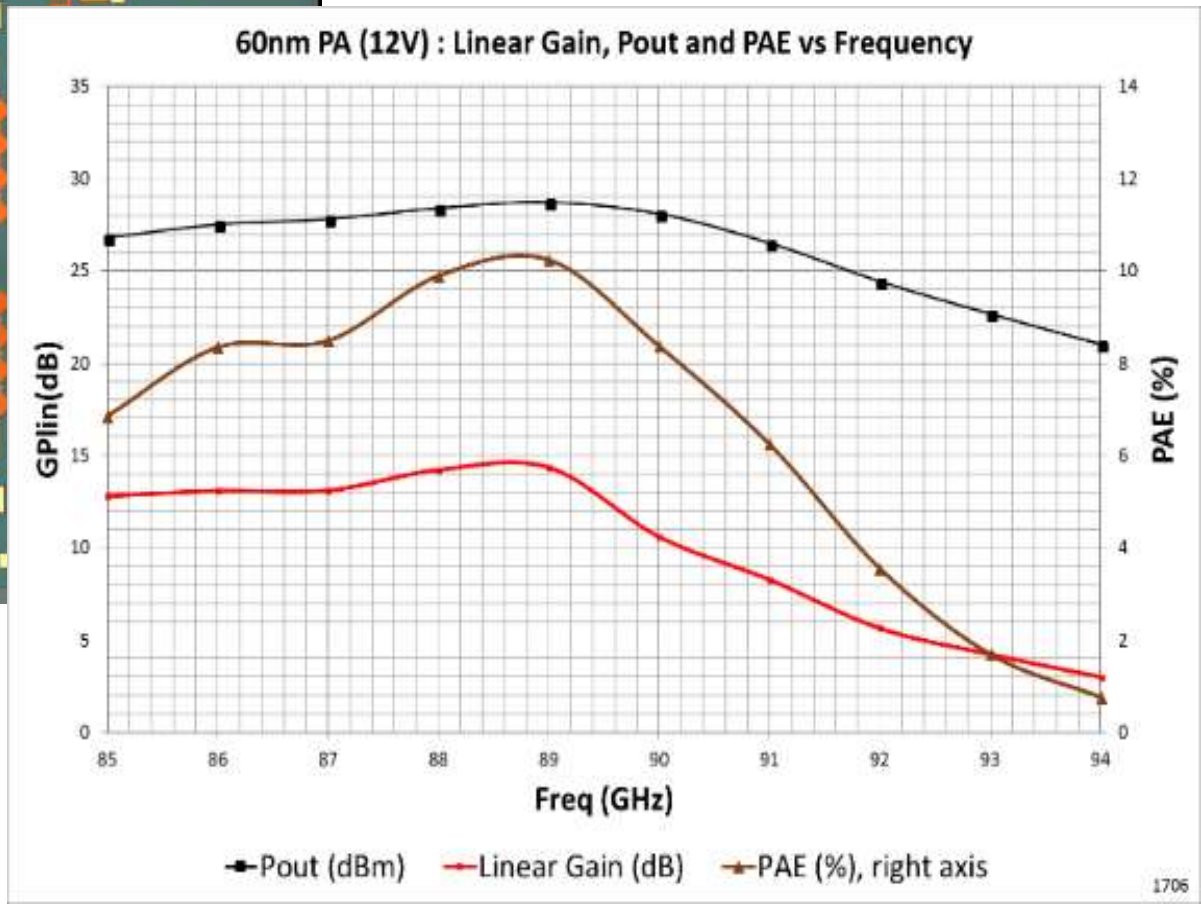
CW test,
in fixture by Erzia



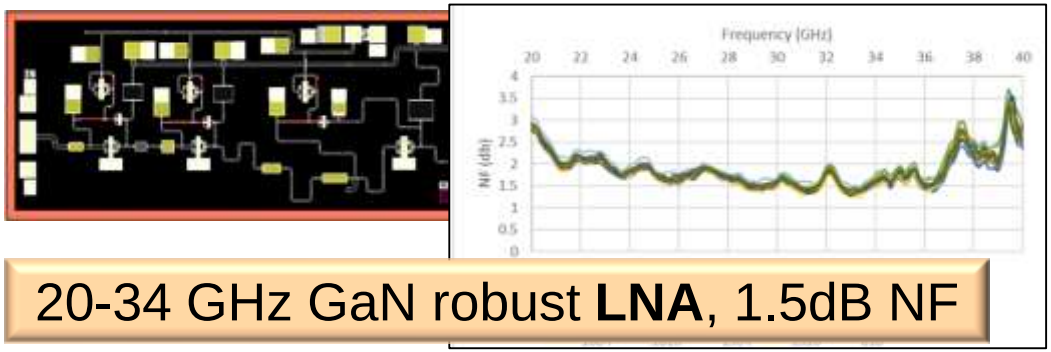
27 dBm 90 GHz PA D006GH (60 nm)



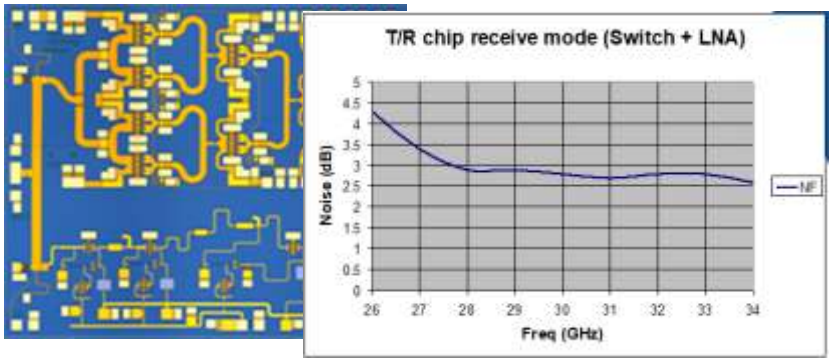
On wafer **CW** test



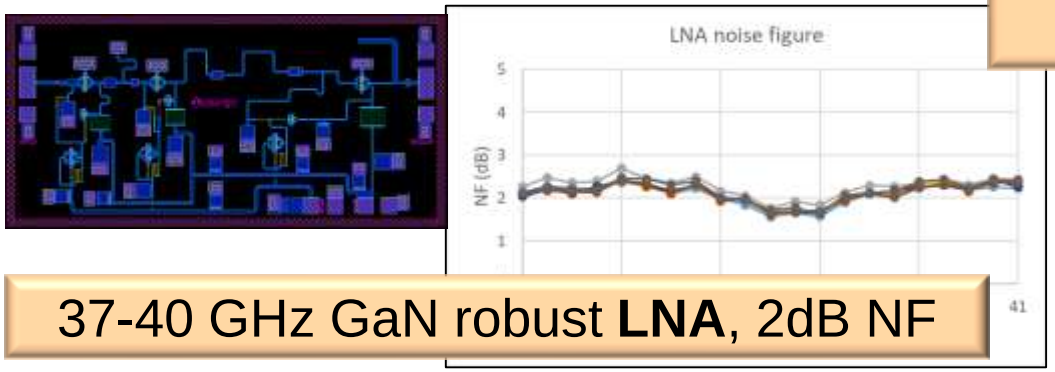
What else ? OMMIC GaN not only for PAs !



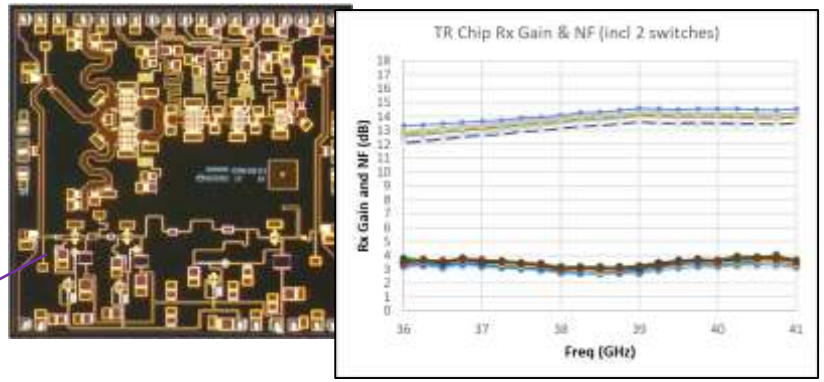
20-34 GHz GaN robust **LNA**, 1.5dB NF



30 GHz TR Chip (**LNA+PA+Switch**)
36 dBm, 2.7 dB NF incl switch



37-40 GHz GaN robust **LNA**, 2dB NF



39 GHz TR Chip (**LNA+PA+2 Switches**)
35 dBm, 3.3 dB NF incl switches

The SERENA project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 779305.

SEREN

Conclusion

- 100 nm and 60 nm GaN/Si microwave process can be used as conventional PHEMT « *but with more power* » for power amplifers from Ku to W band

- With careful design strategy and with the margin given by short gate length, Si allows state of the art performances and excellent reliability with lower cost and less regulation constraints than SiC, opening the possibility of realistic volume production of 5G MMICs at 28GHz, 39GHz and E-band for BackHaul

- The same process presents excellent noise allowing robust LNA products and multifunction SCFE chips

Thank you !