SERENA webinar series Heterogeneous Integration for High Performance mmWave Electronics

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SEREN

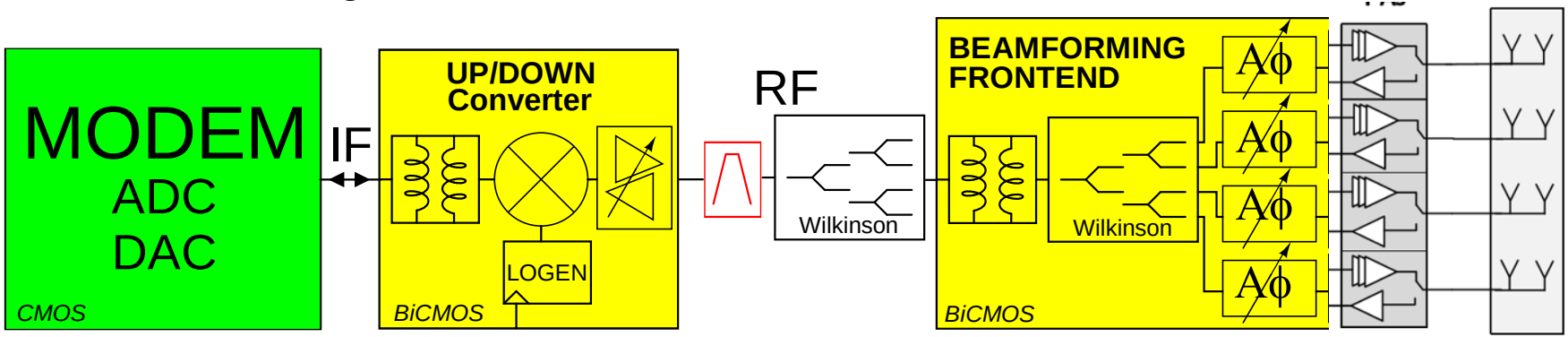
gan-on-**S**ilicon **E**fficient mm-wave eu**R**opean syst**E**m i**N**tegration pl**A**tform

OUTLINE

- Functional split on system level
- RF Technology considerations for Core-chip (RF-beamformer) implementation
- Core-chip design
  - Features
  - Functional block diagram
  - Measured performance
- Summary

System overview / functional split

- Up-down conversion and beamforming split into separate ICs
  - Flexibility
    - RFICs cover all frequency bands
    - External filter adapted to the chosen band
- Quad-channel beamforming RFIC
  - Shortest connections to antennas
  - Effective cooling



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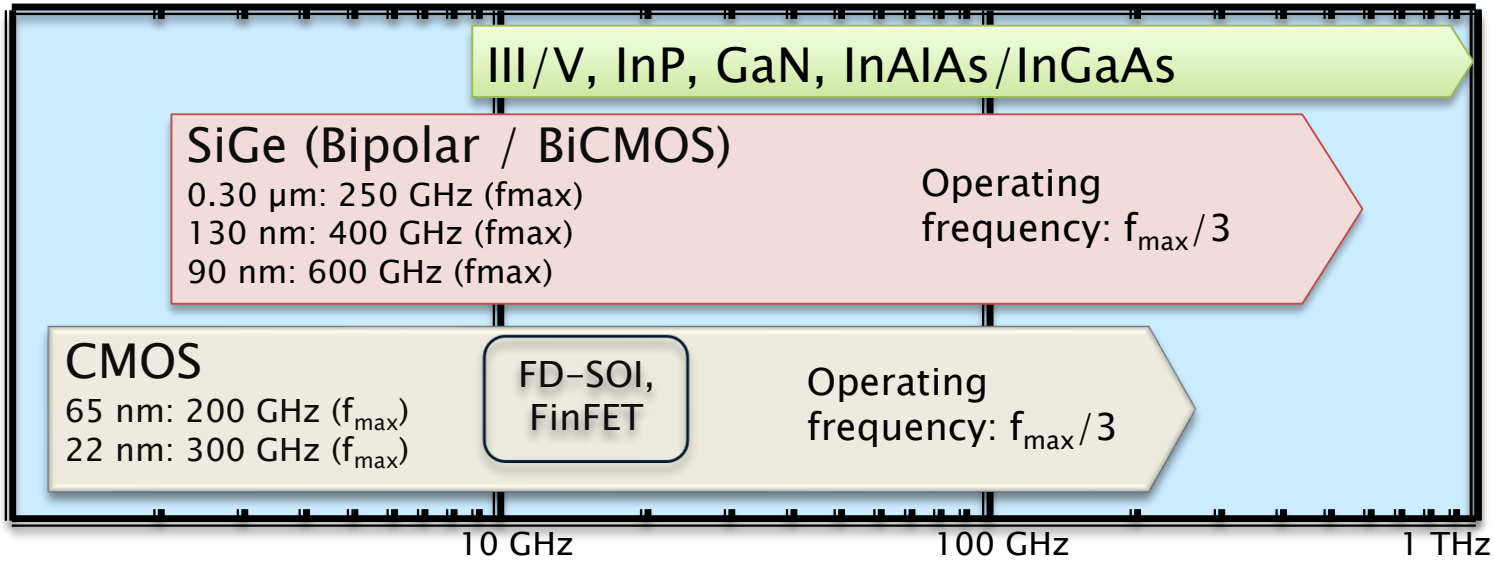
IC Technology Choice – focus on RF

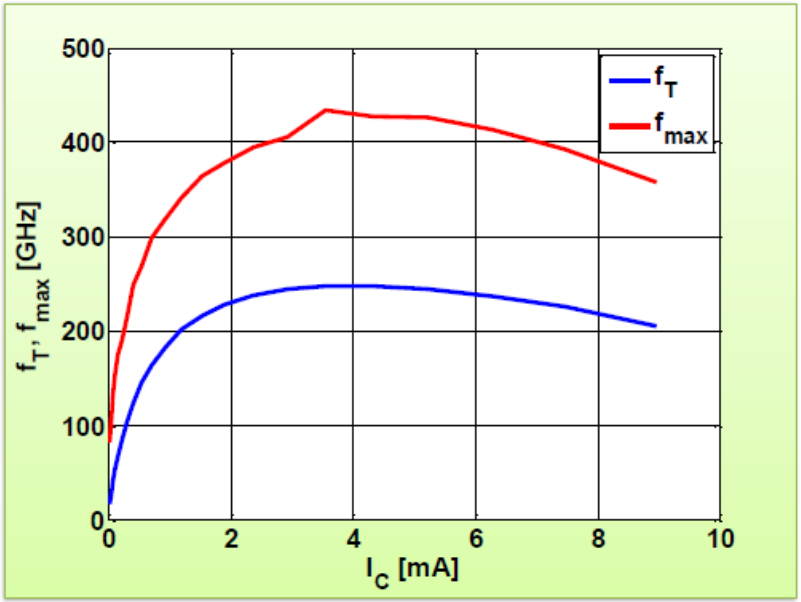


SiGe-HBT: 4x better gm/IDS, Higher voltage (output power), …..

FD-SOI: Dynamical modulation of threshold voltage of devices, ...

GaN HEMT: record power below 100GHz, ...

130nm SiGe-BiCMOS technology features



BV_{ceo}	BV_{cbo}	BV_{ebo}
1,5V	5,3V	2V

130nm SiGe-BiCMOS:
f_{max} = 400 GHz
f_T = 250 GHz
J_C ~ 13 mA/µm²
Min. Gate Delay ~ 2.3 ps
Substrate: p, 20 Ωcm, 8“
Base Layer: SiGe:C
TaN Resistor and MIM-Cap
Metallization:
6 L Copper + 1 L Top Al
(two thick top Cu layers)

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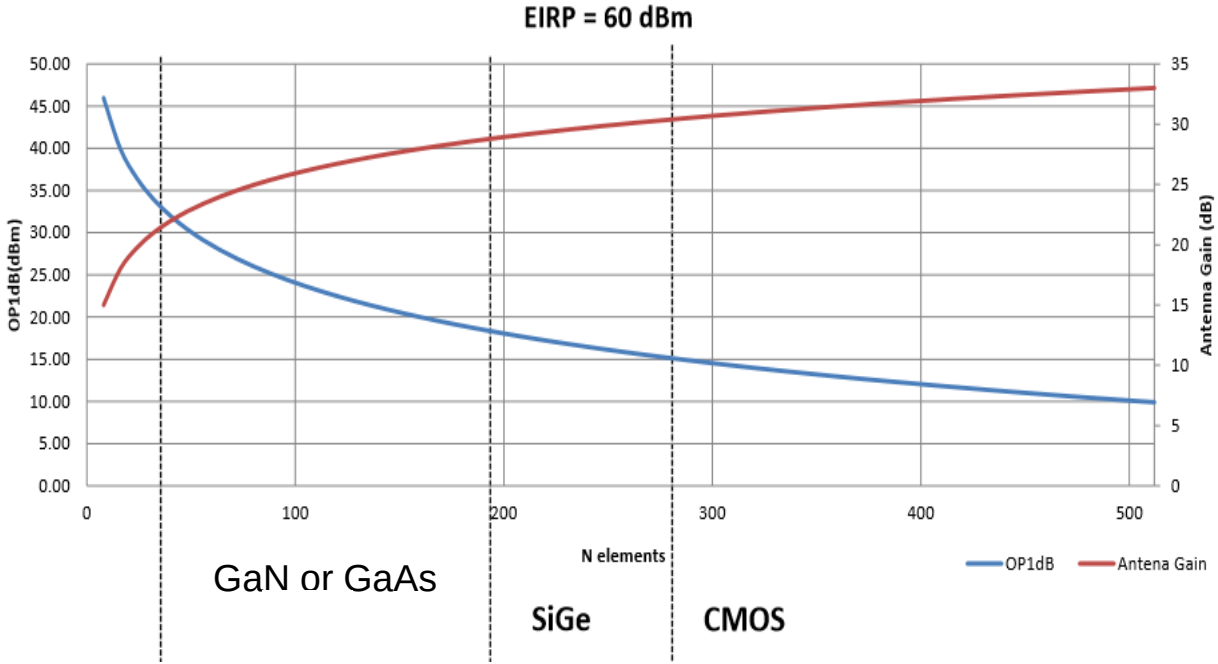
Core Chip Objectives

- Highly integrated SiGe-BiCMOS beamforming RFIC:
  - Quadruple channels
  - Rx/Tx TDD operation
  - 5 Bidirectional RF ports
  - Integrated LNA and PA
  - > 30dB of programmable gain control
  - Full 360° digitally controlled phase shifter (96 states)
  - Fast (< 1µs) digital control using look-up table

Power Amplifier Technology Selection vs. Array Size

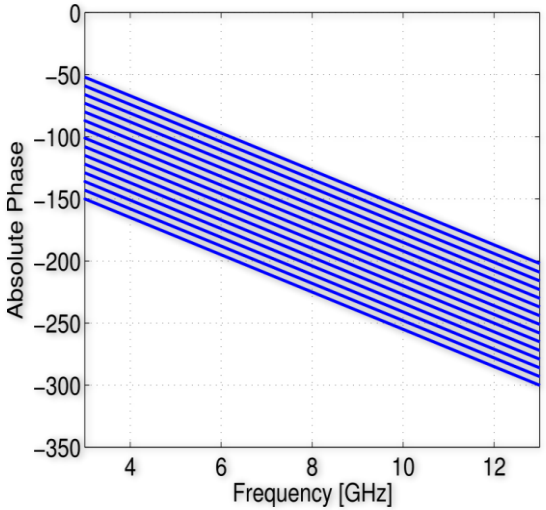
Backoff in the calculation below is 10dB



Phase Shifter versus True Time Delay

Wideband Phase Shifter

(wide carrier frequency range)



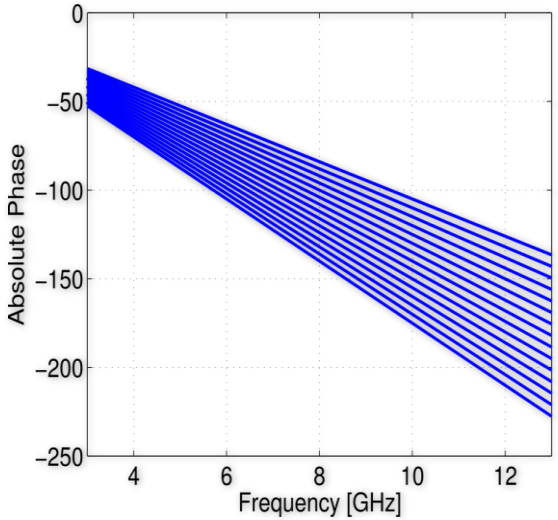
Group Delay

$\phi(x,y)=f(\alpha,\omega,x,y)$

≠

True Time Delay

(wide bandwidth)

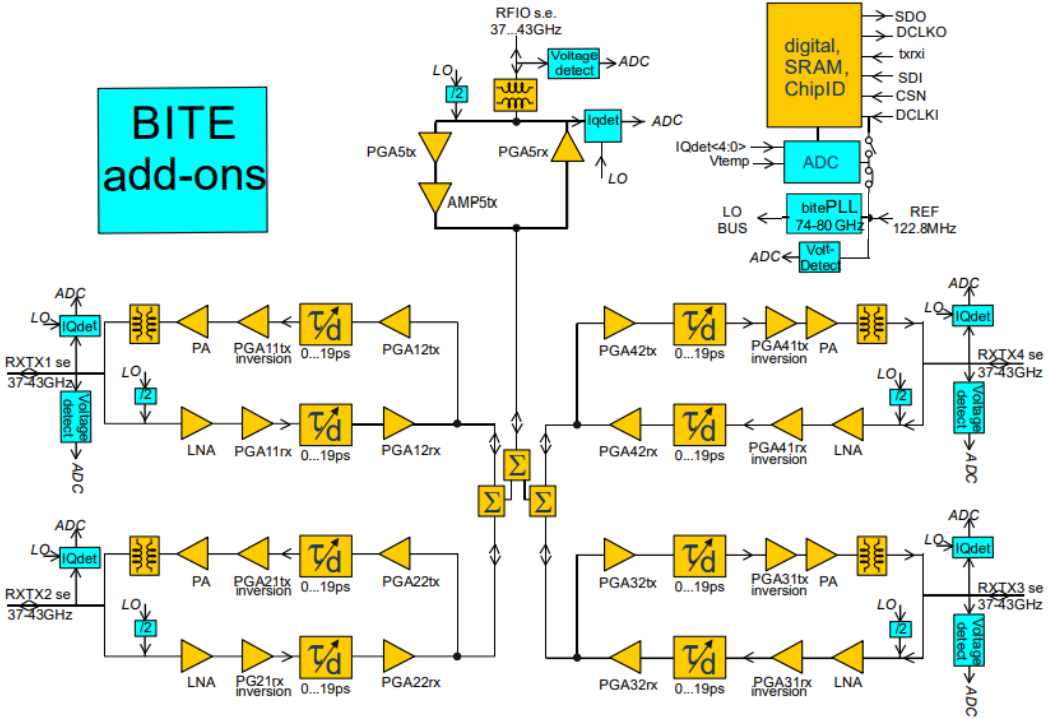


Group Delay

$\tau(x,y)=f(\alpha,x,y)$

- ✓ Variable TTD (instead of variable phase shifter) supports wideband signals.
- × Low-loss, linear, compact RF variable delays are hard to implement.

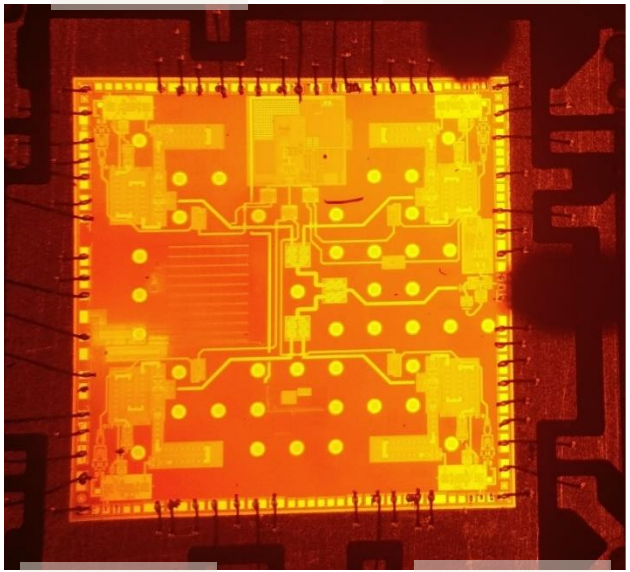
Quadchannel RX/TX 39GHz Beamforming RFIC



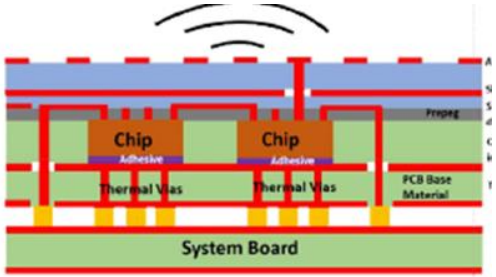
- 37GHz to 43GHz frequency range
- Over 30dB of amplitude control
- Phase/ delay control based on digitally programmable delay lines providing 360° of phase control range or at least 15ps of true time delay control
- RF Built-In Test Equipment including PLL and ADC

Packaging options

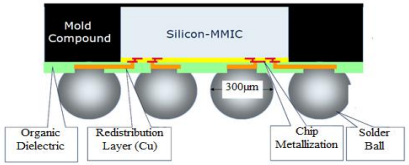
Chip photograph:

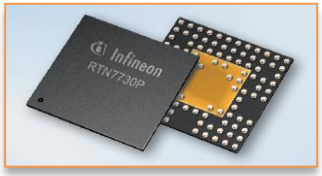


SERENA:
Packaging by 'Chip-Embedding' and AiP



eWLB (embedded Wafer Level Ballgrid-Array) Packaging





RFIC small signal performance

TRANSMIT

Max gain and max delay configuration

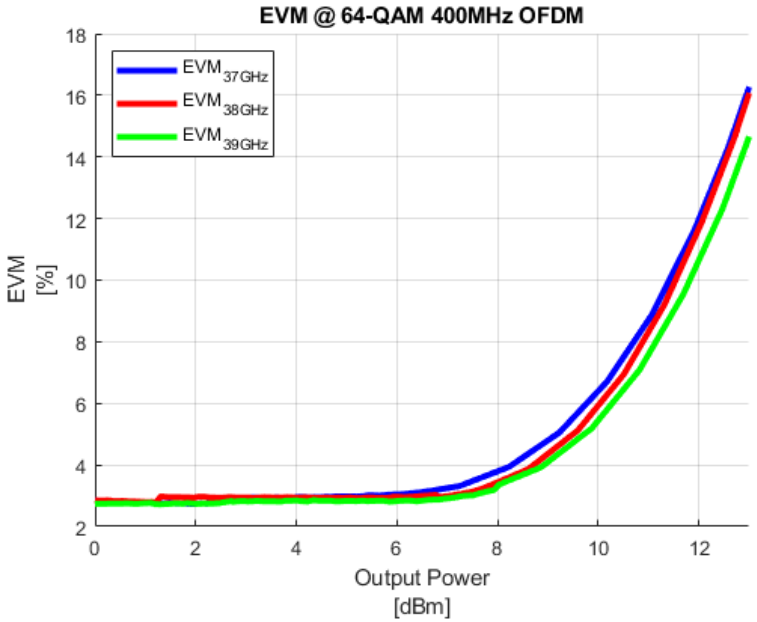
- Gain>32dB over 37GHz - 43GHz
- Peak gain of 38dB
- Input matching better -15dB over 37GHz – 43GHz
- Output matching better -10dB over 37GHz – 43GHz

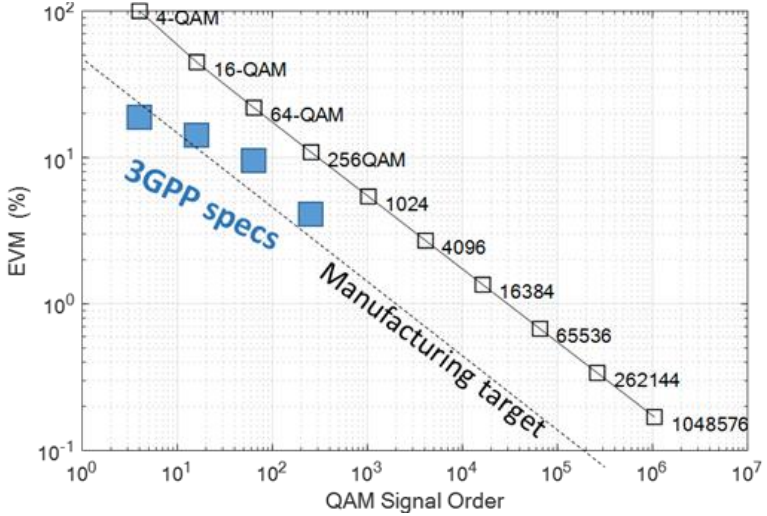
RECEIVE

Max gain and max delay configuration

- Peak gain of 10dB
- Input/output matching better -12dB over 37GHz – 43GHz
- NF of <6dB at ambient temperature

EVM measurements

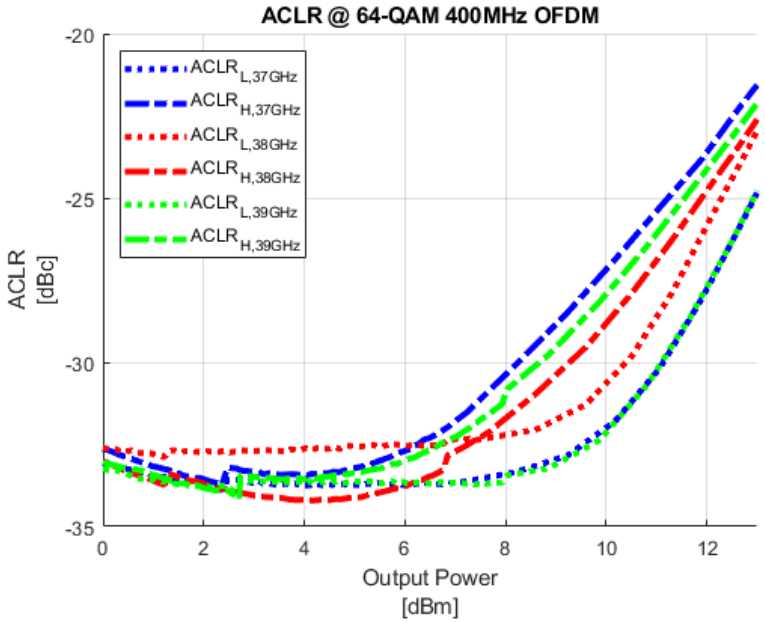




EVM Required to Support Different Orders of Modulation, as Extrapolated from 3GPP Metrics

Courtesy of Earl McCune

ACLR measurements



Establishing translations between circuit and radiated performance is challenging

Beamforming and AAS/massive MIMO implies new challenges due to e.g. antenna cross talk etc.

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Summary

- SiGe-BiCMOS is a performance and cost efficient technology for this application
- Low-loss, linear and digitally programmable delay lines successfully implemented
- Integrated BITE is very useful for circuit-test and calibration
- PA becomes the bottleneck and has to be addressed at all levels including technology selection and architecture
  Significant improvement needed for volume deployment
  (like fineline GaN technology, Doherty PA with RF predistortion, Relaxed ACLR specification, …)

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