SERENA H2020 PROJECT

Heterogeneous Integration for High Performance mmWave Electronics

IZM Serena Team
Fraunhofer IZM

ivan.ndip@izm.fraunhofer.de

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SEREN

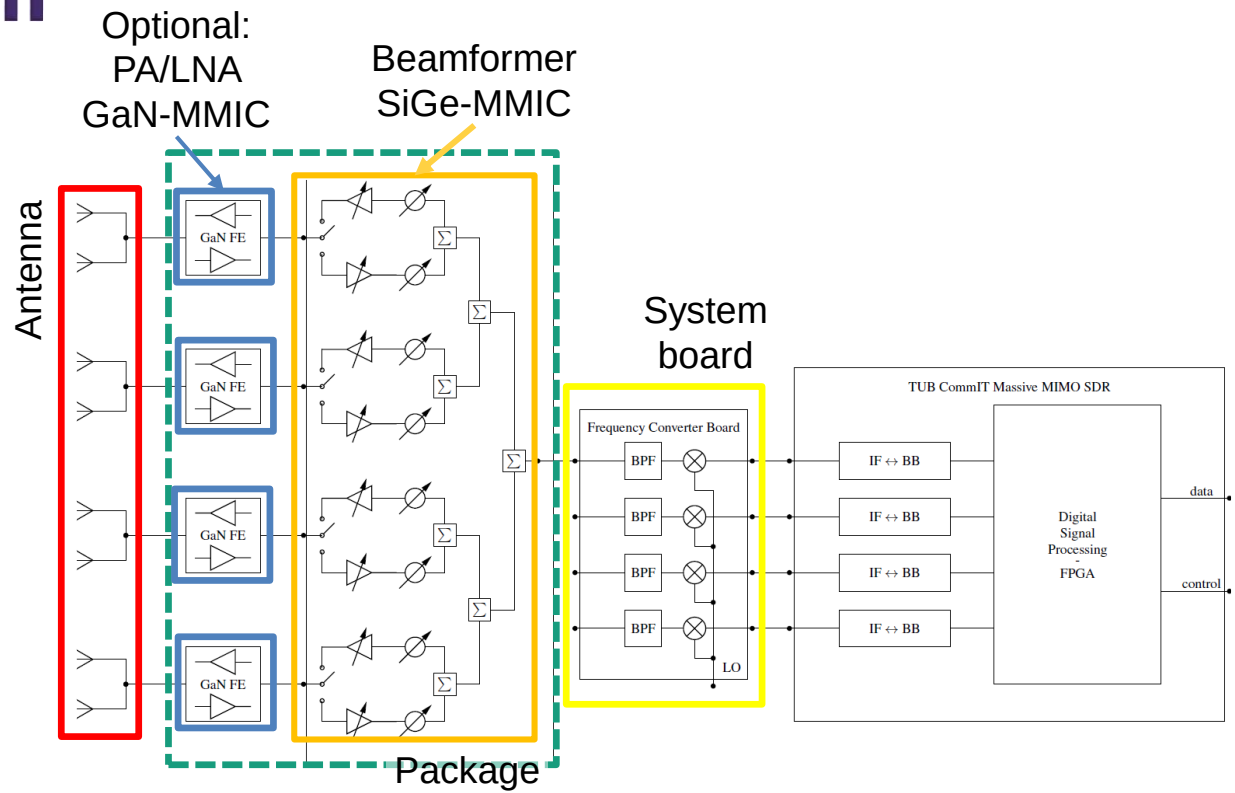
gan-on-**S**ilicon **E**fficient mm-wave eu**R**opean syst**E**m i**N**tegration pl**A**tform

Outline

- Specification / Block diagram
- Package concept, substrate stack-up
- Material characterization
- Design of module and components
- Fabrication
- Measurement

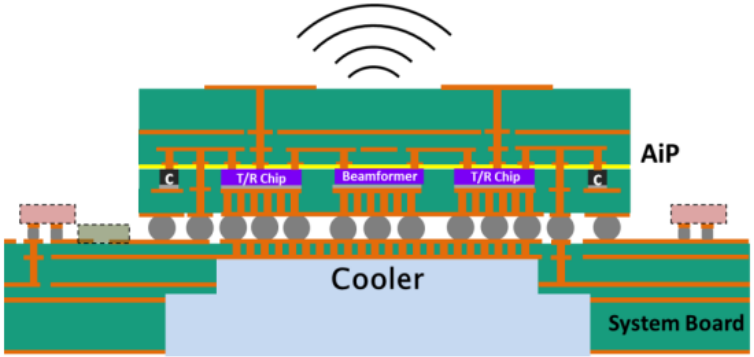
Block Diagram

- Hybrid Beamforming demonstration system for 5G base stations
- Antenna-in package RF front-end
- Integration of
  - GaN PA/LNA
  - SiGe beamforming MMICs



Package Concept

- Embedding Antenna-in-Package module
- Infineon Beamer IC 39 GHz + 100 pF decoupling capacitors (for each VDD pin)
- 6 metal layers
- L2 and L3 for redistribution - keepout above IC
- Antenna ground plane on L1
- Bottom layer for LGA Interface



European Patent Nr. EP3346548B1; US20180191062A1

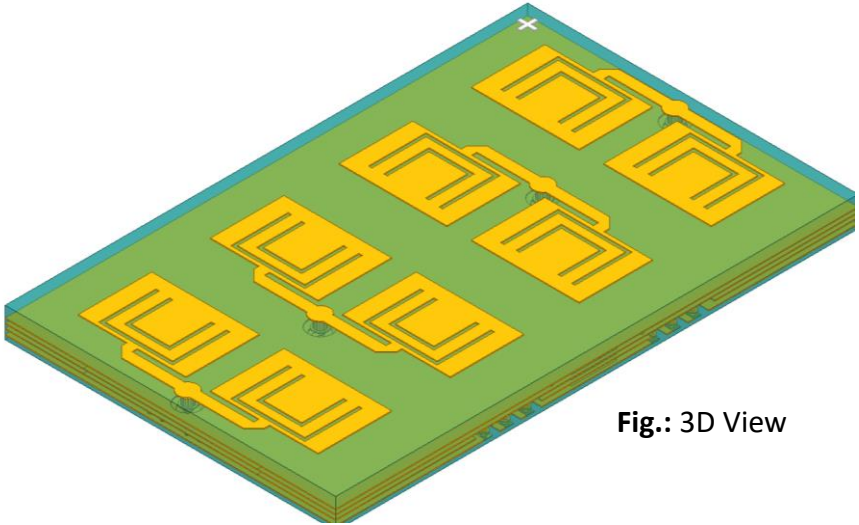
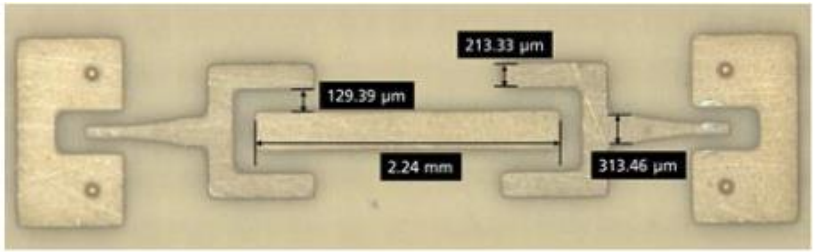


Fig.: 3D View

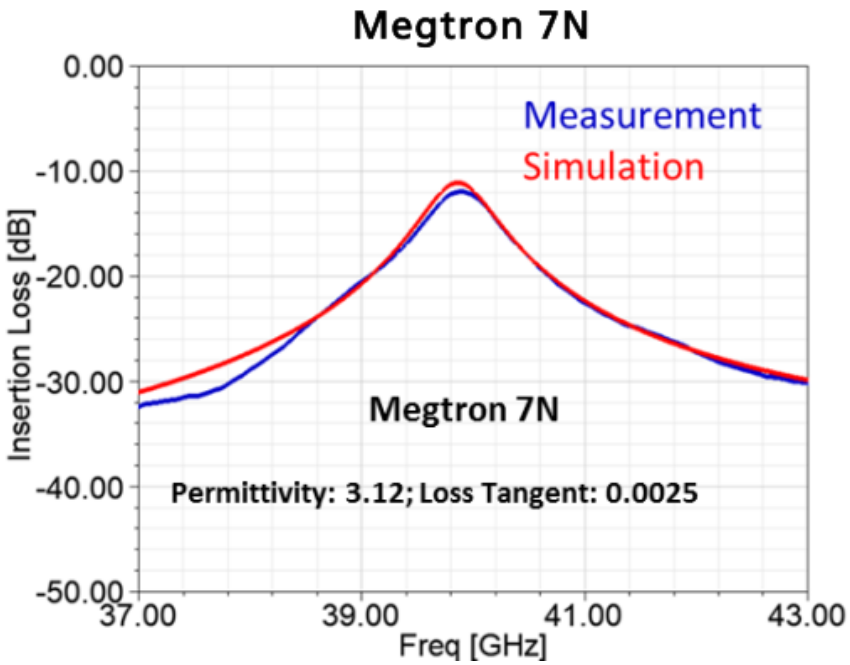
Fig.: Concept of SERNA module

Dielectric Material Characterization

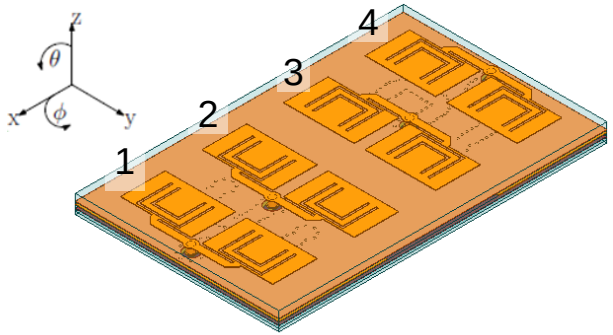
- Dieelctric material characterization using planar resonators

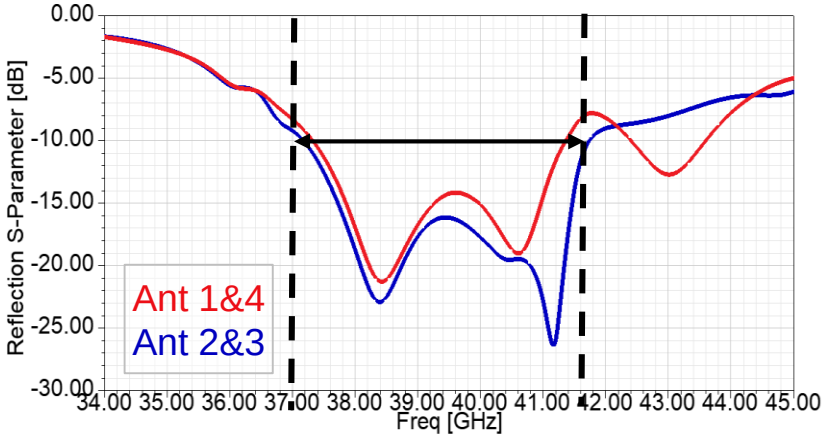


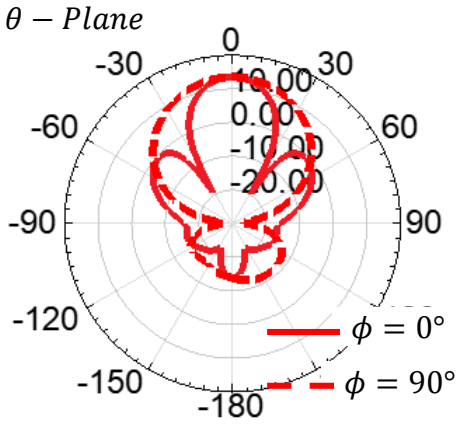
Fabricated planar resonator for measuring relative dielectric constant and loss tangent of Megtron 7N substrate



Package Component Design - Antennas



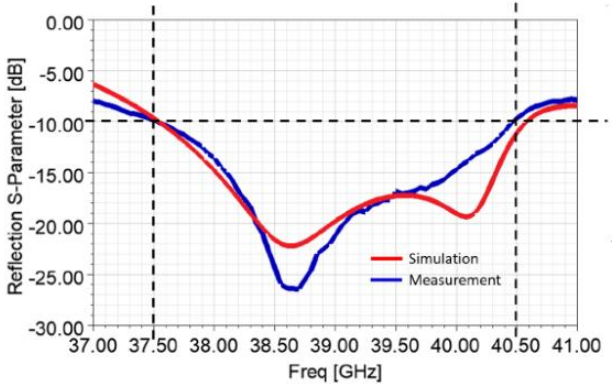


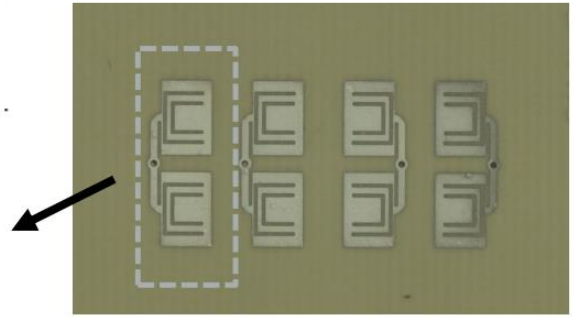


Antenna properties

- -10 dB bandwidth
  - Antenna 1&4: 4 GHz (37.3-41.3 GHz)
  - Antenna 2&3: 4.5 GHz (37.1-41.6 GHz)
- Realized gain (full array): 13.5dBi @ 38.5 GHz

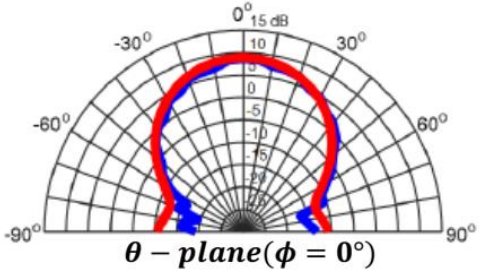
Package Component Design – Antennas



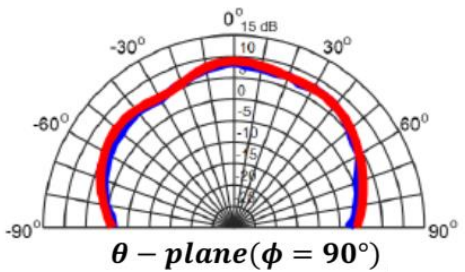


Fabricated antenna array

Parameter	Simulation	Measurement
Bandwidth	3 GHz (37.5 GHz – 40.5 GHz)	3.1 GHz (37 GHz – 40.6 GHz)
Peak Gain	9 dBi	8.8 dBi



$\boldsymbol{\theta - plane(\phi = 0°)}$



$\boldsymbol{\theta - plane(\phi = 90°)}$

Package Design Board-IC Interconnect

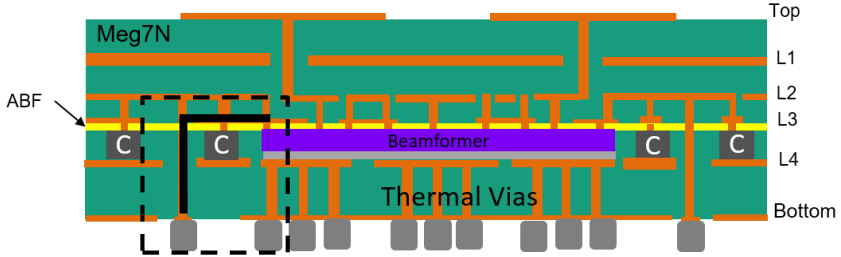


Fig.: Stackup of the SERENA modules

Module: GCPW
- Width: 110 µm
- Slot: 150 µm

System board: SL
- Width: 137 µm

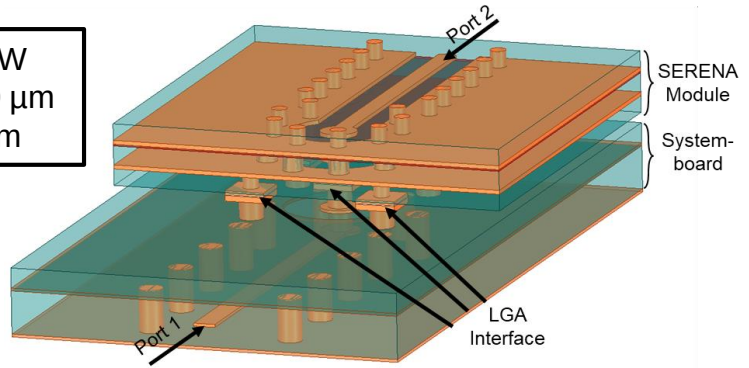


Fig.: LGA transition from systemboard to SERENA embedded module

Package Design IC-Antenna Interconnect

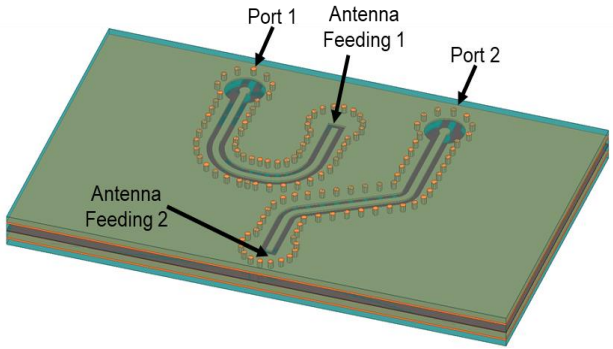
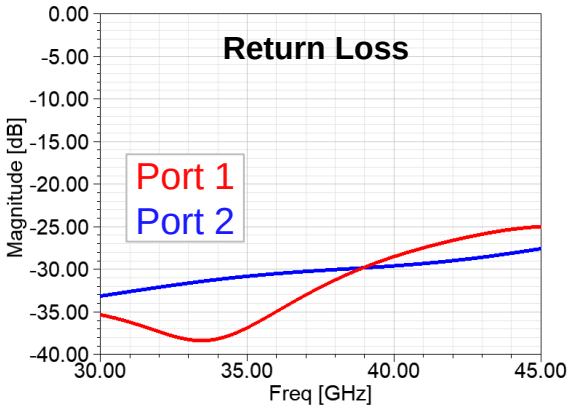
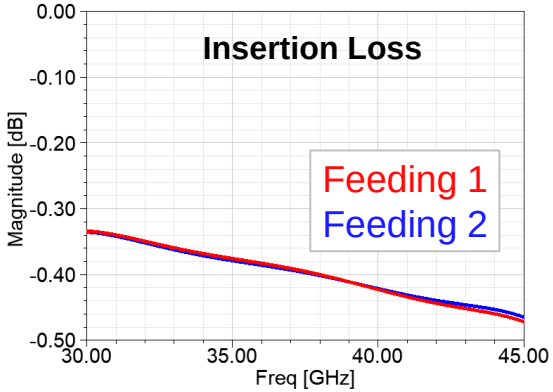
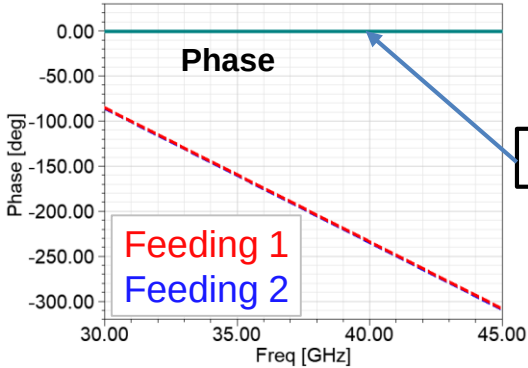


Fig.: Transmission lines from chip to antenna on layers L3 and L4 in the low power module.







$\Delta_{phase} \approx 0.79$ deg

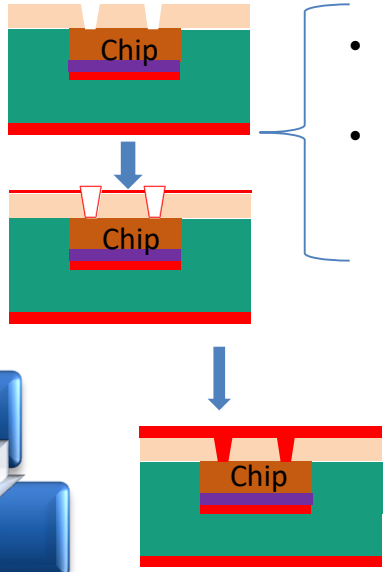
Layer 4: GCPW
- Width: 123 µm
- Slot: 100 µm

Layer 3: GCPW
- Width: 110 µm
- Slot: 150 µm

Total length: ≈ 6 mm

Fabrication – Embedding Process

- Die placement (sinter glue)
- Embedding process Megtron 7N + ABF
- Laser drilling
- Sputtering process
- Electro plating



- sputtering process (plating base): 100nm TiW / 300nm Cu
- important: degassing of substrate prior to sputter process in order to ensure better Cu adhesion

electro plating: special electro plating bath with leveling characteristic (“via filling”)

Fabrication - Lamination

- After embedding follows the build-up of the 3 further routing layers above the embedded layer

- Main process steps for each layer:
  - lamination
  - laser drilling
  - metallization
  - structuring
  - pre-treatment for next lamination step

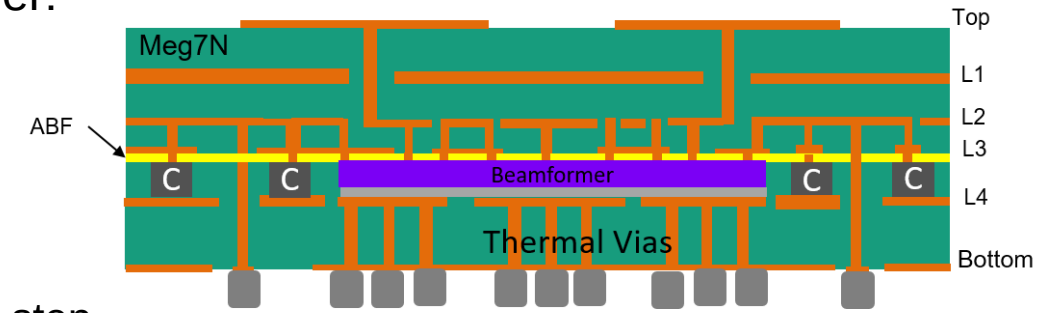
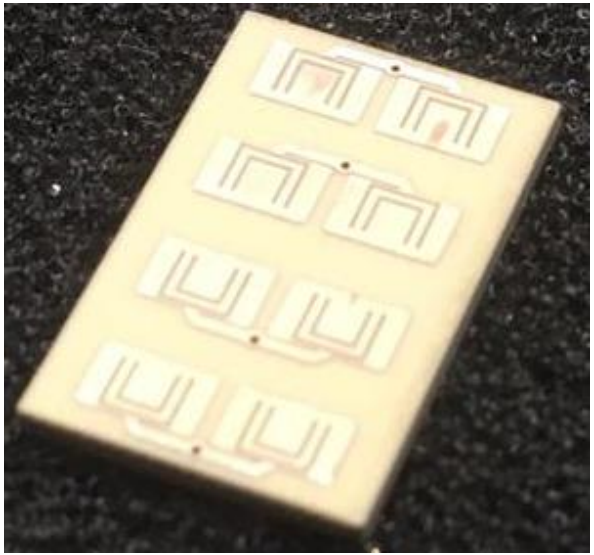


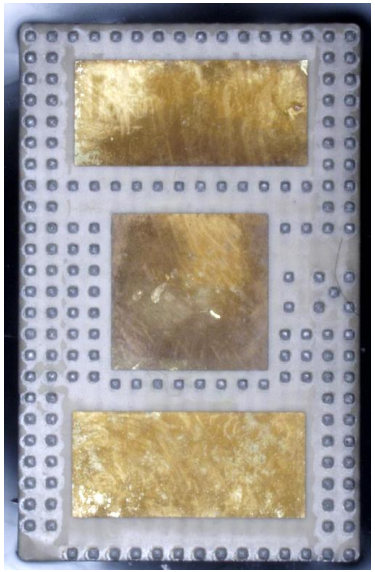
Fig.: Stackup of the SERENA module

Fabricated Module

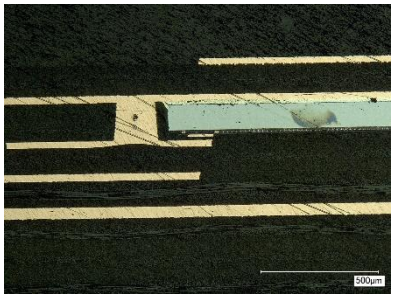
Top: Antenna layer



Bottom: LGA layer



Cross sections



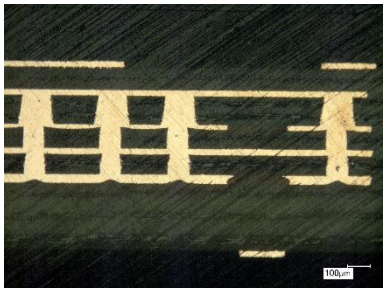


Fig.: Fabricated Low power module.

Fabricated Modules - X-ray

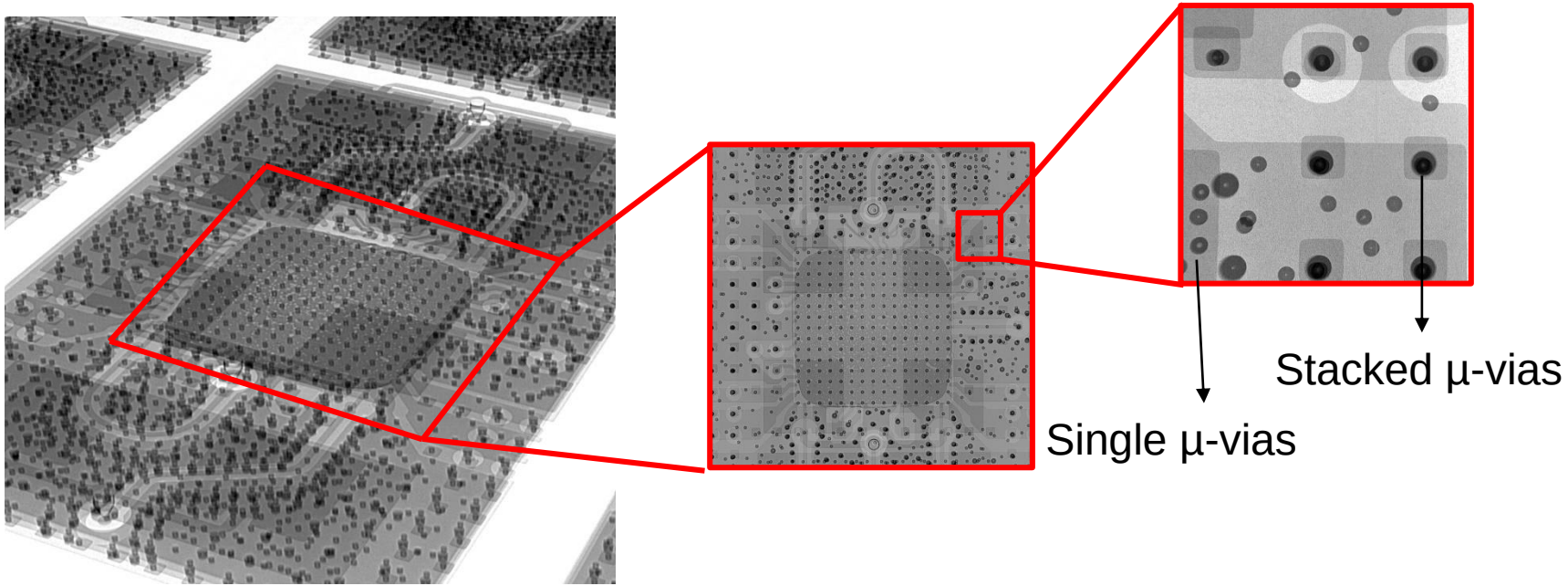


Fig.: X Ray - Fabricated Low power module.

RF Characterization Set-up

- Embedding test structure with GaN PA/LNA IC
- On-wafer characterisation
  - Connected to PNA E8361A (20 – 55 GHz)
  - DC block on port 1
  - Tests on bare dies and assembled ICs
  - OMMIC recommends to keep I_D to 63 mA by tuning V_S

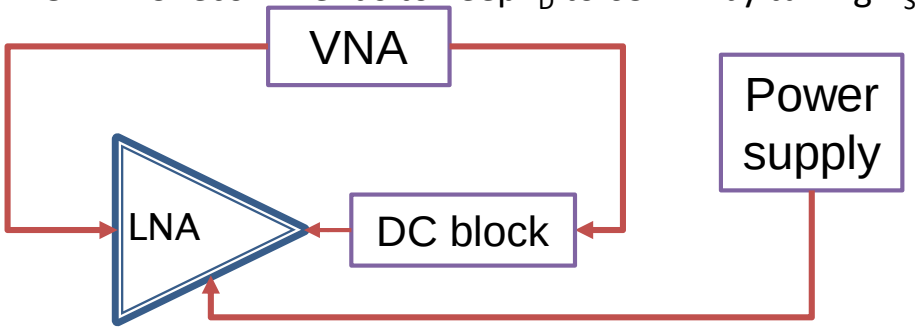


Fig.: Block diagramm of setup for RF measurements.

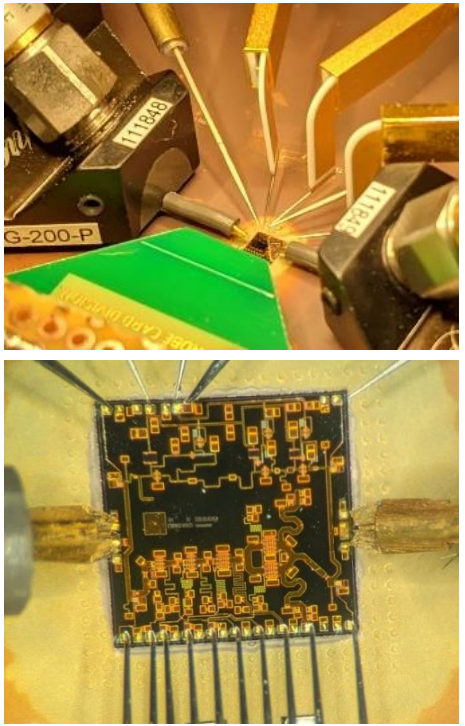
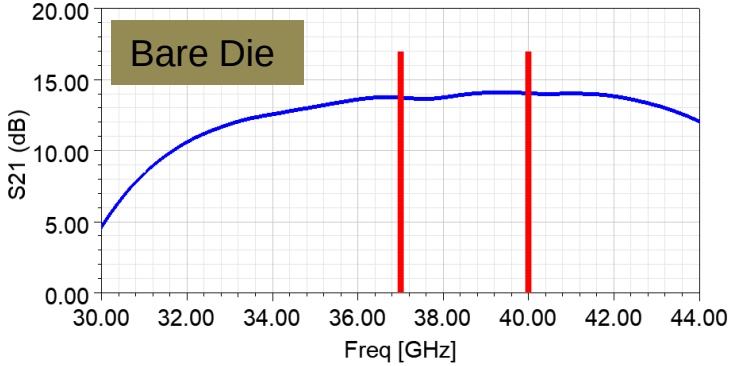
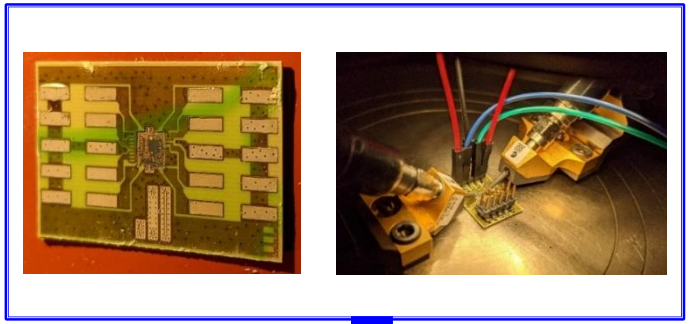
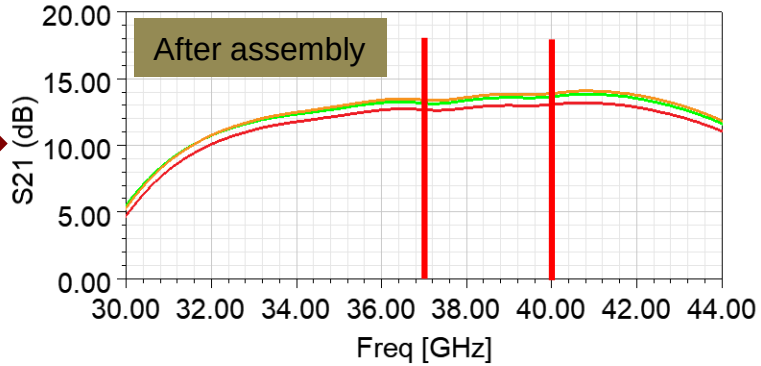


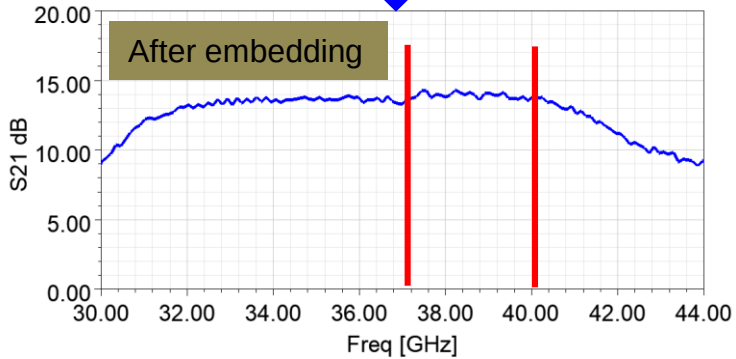
Fig.: Setup for probe measurements.

RF Characterization – GaN LNA









Evaluation of Fabricated Modules (Non-destructive Testing)

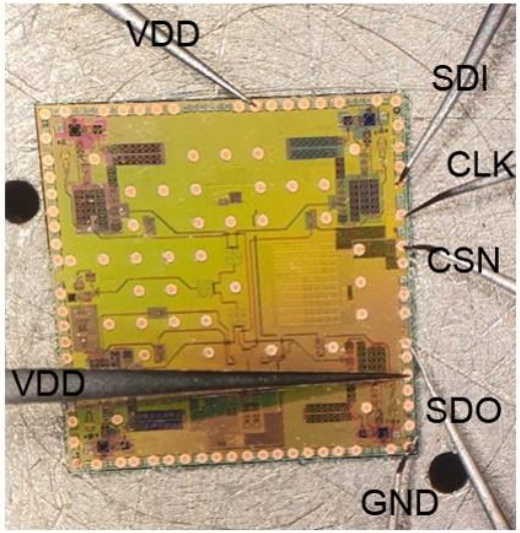


Fig.: Bare-die measurement

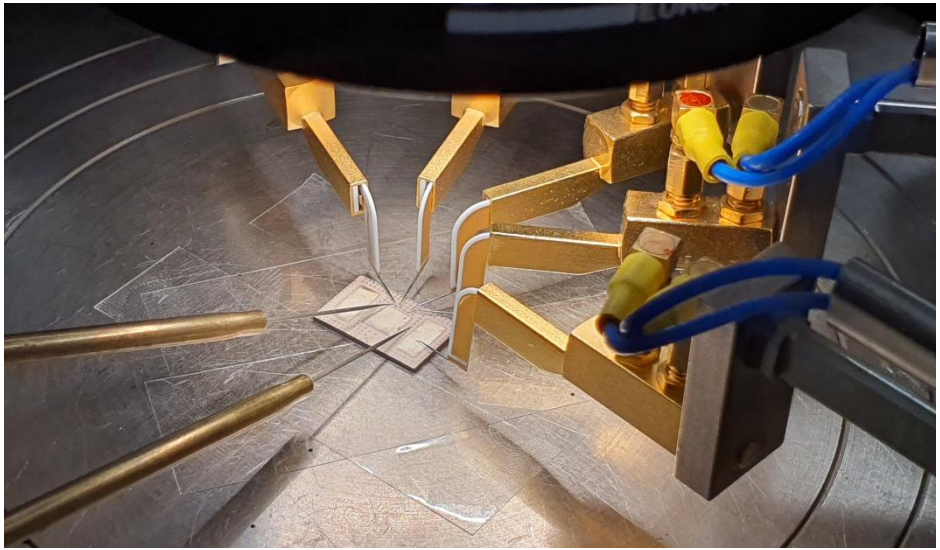


Fig.: Probed measurement on a module

Evaluation of Fabricated Modules (Non-destructive Testing)

```
test 1/6
checking BEAM39PA status
this should print "status (0x4080): PON LOCK" after power on and "status (0x0000):" after reruning this test
**
M1B1: status (0x4100): PON
**
clearing and checking BEAM39PA status, this should print "status (0x0000):"
cleared status registers
**
M1B1: status (0x0000):
**
reseting all BEAM39PAs to be in a known state: resetting SERENA system
press enter to continue, ctrl+c to stop

test 2/6
testing register read/write of the BEAM39PA
This test uses the register PLL_CTRL_1. It tests for the default value, writes a value and reads it back.
testing BEAM39PA M1B1
  reading default value:
  * reading successful, default value wrong
  writing test value
  reading test value:
  * reading successful, value wrong
  writing back default value
press enter to continue, ctrl+c to stop

test 3/6
testing BITE power (ADC), this should increase the current drawn at the VDD pin by probably >10mA
testing BEAM39PA M1B1
  press enter to enable the ADC
  * ADC enabled
  press enter disable the ADC
press enter to continue, ctrl+c to stop

test 4/6
testing RF power, VDDPA supply required.
Are the VDDPA pins and all VDD pins connected? Press "y" and enter for yes, just enter for no:
skipping RF power test.
press enter to continue, ctrl+c to stop

test 5/6
running MBIST tests of the BEAM39PAs, this should print "MBIST test successful"
  * Error using MmdSerenaBeamer/run_mbist (line 2532)
M1B1: error reading MBIST result or not done, code 0, mbist reg FF20
```

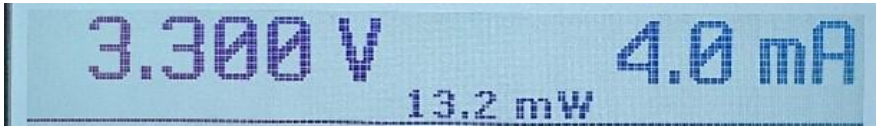


Fig.: Results of Bare-die & Probed module measurement

Evaluation of Fabricated Modules (Destructive Testing)

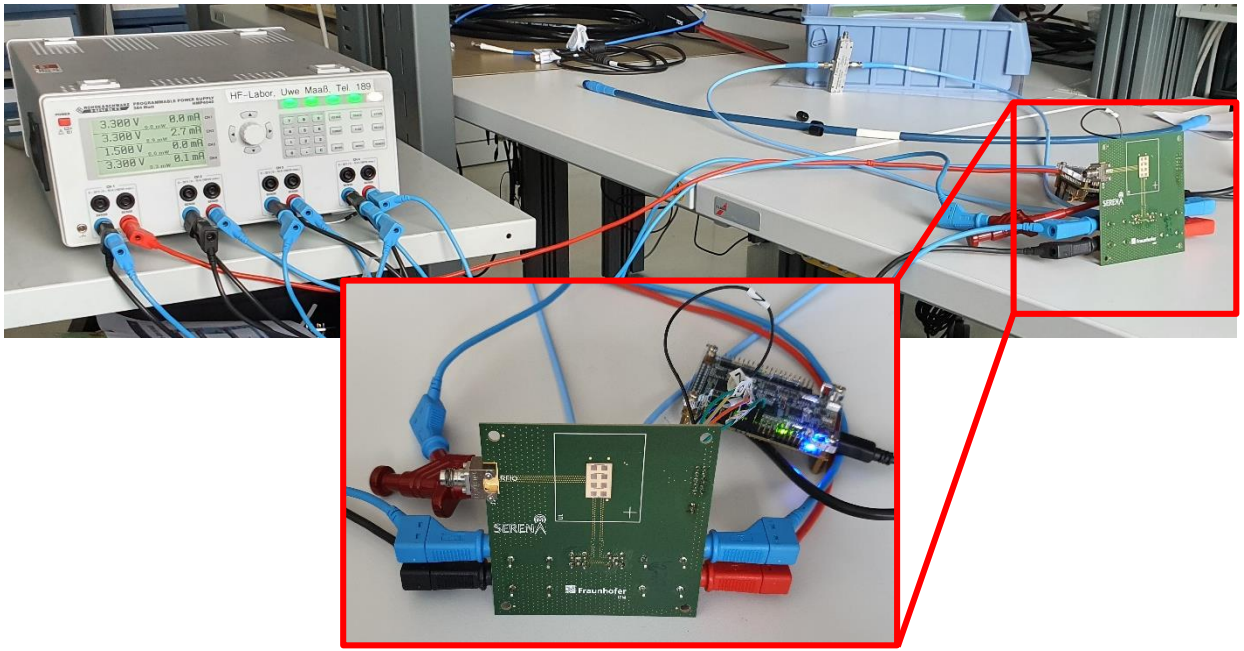


Fig.: Measurement set-up of module mounted on test board including SPI interface

Evaluation of Fabricated Modules (Destructive Testing)

```
test 1/6
checking BEAM39PA status
this should print "status (0x4080): PON LOCK" after power on and "status (0x0000):" after reruning this test
**
M1B1: status (0x4080): PON LOCK
**
clearing and checking BEAM39PA status, this should print "status (0x0000):"
cleared status registers
**
M1B1: status (0x0000):
**
reseting all BEAM39PAs to be in a known state: resetting SERENA system
press enter to continue, ctrl+c to stoptest

2/6
testing register read/write of the BEAM39PA
This test uses the register PLL_CTRL_1. It tests for the default value, writes a value and reads it back.
testing BEAM39PA M1B1
  reading default value:
  * reading successful, default value correct
  writing test value
  reading test value:
  * reading successful, value correct
  writing back default value
press enter to continue, ctrl+c to stop test

3/6
testing BITE power (ADC), this should increase the current drawn at the VDD pin by probably >10mA
testing BEAM39PA M1B1
  press enter to enable the ADC
  * ADC enabled
  press enter disable the ADC
press enter to continue, ctrl+c to stoptest

4/6
testing RF power, VDDPA supply required.
Are the VDDPA pins and all VDD pins connected? Press "y" and enter for yes, just enter for no:
 ypowering up the common channel and channel 0 in RX mode, current drawing should increase by roughly 120mA.
testing BEAM39PA M1B1
  press enter to power common channel and channel 0 up
  * M1B1: powered up  press enter to power common channel and channel 0 down again
  * M1B1: powered down
press enter to continue, ctrl+c to stoptest

5/6
running MBIST tests of the BEAM39PAs, this should print "MBIST test successful"
  * M1B1: MBIST test successful
press enter to continue, ctrl+c to stoptest
```

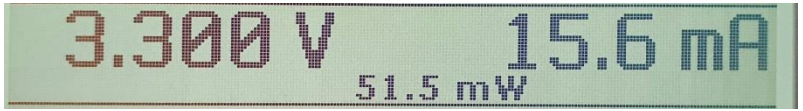


Fig.: Results of mounted module measurement on test board

Summary

- Extraction of material properties
- Design of antenna and interconnect elements
- Embedding of ICs and embedded capacitors
- Fabrication of Module
- Successful testing of the module

SERENA Grant Agreement No. 779305

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If you need further information, please contact the coordinator:

TECHNIKON Forschungs- und Planungsgesellschaft mbH
Burgplatz 3a, 9500 Villach, AUSTRIA
Tel: +43 4242 233 55 Fax: +43 4242 233 55 77
E-Mail: coordination@serena-h2020.eu