Artificial Intelligence
5G
Energy Efficiency
Enabling best-in-class GaN-on-Si devices for 5G: epitaxy
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SERENA EU project – Webinar November 4th, 2021
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Outline

1. GaN-on-Si: an innovation enabler for RF
2. The differentiating features of Soitec's GaN technology at the bottom of the SERENA project
3. Summary

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GaN – an innovation enabler in the RF market

Soitec products portfolio mobile communications

APPLICATIONS

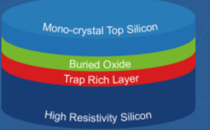
- Smartphones radio-frequency front-end modules
- Networking base stations

SOITEC PRODUCTS ENABLE

- 4G
- 5G
- WiFi 6 connectivity

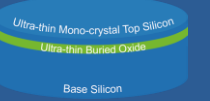
RF-SOI

For highly efficient mobile communication



FD-SOI

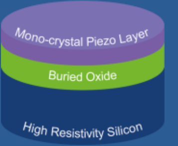
Integrated technology



POI

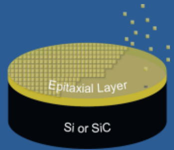
High performance

5G filters

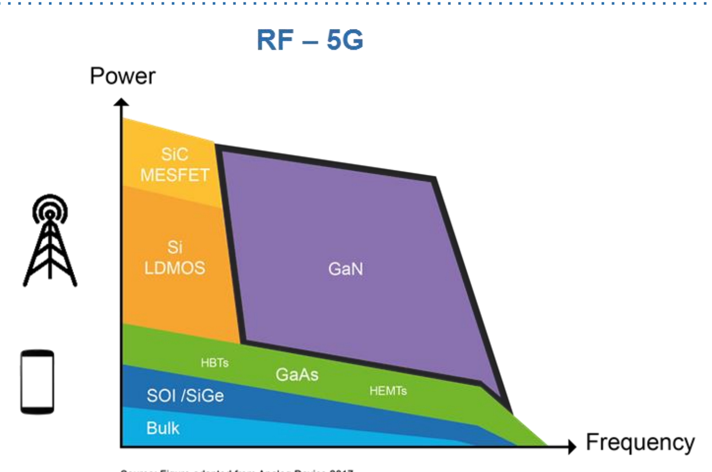


GaN

High performance power amplifier



GaN epitaxial wafers - enabling technology for 5G



- **Cellular base stations (>5W power amplifier)**
  - GaN - becoming mainstream for 4G / 5G <6GHz and mmW
- **Cellular handset (<3W Power amplifier)**
  - GaAs – mainstream technology for 4G / 5G <6GHz
  - GaN – advantage for 5G mmW

Market outlook

EpiGaN SAM in CY26
~300 k wafers (150mm eq.)

Future opportunities on power automotive & sensors

RF GaN/Si - an attractive technology for 5G mmwave

Technology Criteria	RF GaN/Si proof points	Demos, chip designs, data
Economies of Scale	✓ 150mm, 200mm GaN/Si epiwafers available in volume today ✓ 300mm GaN/Si technology in development ✓ Compatible with Si CMOS fab	
Integration	✓ 30GHz GaN/Si transceiver MMIC with integrated 4W PA, LNA and switch	PA, SPDT, Ant, TxIN, RxOUT, LNA Figure 7b: Ka band Transmit/Receive chip photograph Source: OMMIC
Bandwidth, Frequency	✓ Wide bandwidth performance, single PA covering multiple bands ✓ From 5G (sub6, mmW) to 6G bands	14-18GHz 20W GaN/Si PA 94-100GHz 0.5W GaN/Si PA Source: MC2, OMMIC
High or Low Voltage Operation possible - associated to highest PAE	✓ High Breakdown Voltage (VDS>28-50V) ✓ Low supply (knee) voltage due to • Ultra-low Rs GaN HEMTs (e.g InAlN <250 Ohm/sq) & • Low ohmic contact resistance (**ohmic regrowth by MOCVD**) ✓ Significantly improved **PAE** for all 5G bands with GaN (e.g. longer battery life times)	300mm GaN (this work), GaAs (≤100mm), Si/SOI, PAE +20%, +6%, 45% Better than Si; Sat. PAE (%), Frequency (GHz); f=5GHz, f=28GHz, PAE (%), P_L (dBm) Source: Intel

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The differentiating features of Soitec's GaN technology at the bottom of the SERENA project

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Soitec's GaN epitaxial current product offering

RF

GaN - on - SiC

(In,Al,Ga)N epi active layers
GaN RF Buffer
HR-SiC

- 100 & 150 mm
- Sub-6GHz or mmwave

GaN - on - Si

(In,Al,Ga)N epi active layers
GaN RF Buffer
HR-Si

- 150 & 200 mm
- Sub-6GHz or mmwave

Power Amplifiers & Front-ends

Infrastructure & Handsets

Power

GaN - on - Si

AlGaN epi active layers
HV GaN epi Buffer
CZ-Si

- 200 mm
- Discrete HEMTs or ICs
- Normally-on or normally-off
- 200V or 650V

GaN - on - SOI

AlGaN epi active layers
HV GaN epi Buffer
SOI

- 200 mm
- ICs and SoCs
- Normally-on or normally-off
- 200V or 650V

under development

Efficient Power

Power supply, fast chargers

EV Automotive

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Soitec's RF GaN products provide differentiation for 5G

In-situ SiN, optional GaN cap

In-situ SiN as a high-quality gate dielectric, robust surface passivation

Optimized heterostructures available

- AlGaN/SiN or AlGaN/GaN for sub6GHz
- AlN/SiN, InAlN for mmW bands

State-of-the-art Fe-free RF buffers

excellent DC resistivity&breakdown, RF losses and dynamic performance

On Silicon or SiC substrates

up to 200mm Si, up to 150mm SiC

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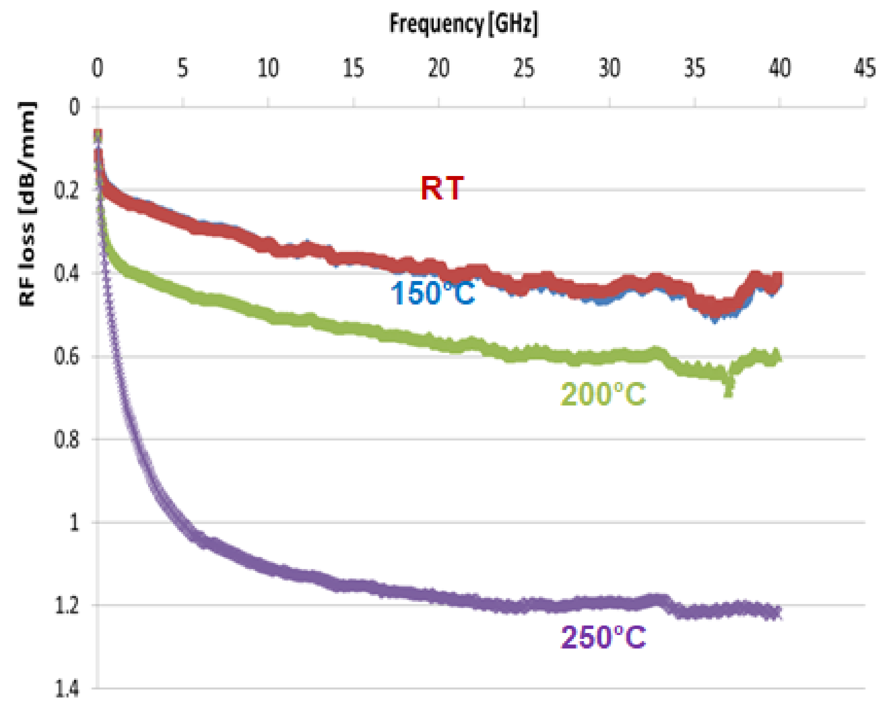
High Temperature assessment of RF losses in GaN/Si

- Losses for GaN-on-Si are very comparable to GaN-on-SiC up to 20 GHz
- Losses remain low (< 0.8 dB/mm) up to 100 GHz!
- on 200 mm HR CZ- Si(111)



RF losses remain below 1db/mm up to **200°C**

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DC Breakdown Voltage Material

- Lateral Breakdown Voltage: Ec ~ 1MV/cm
- Leakage current <1uA/mm until device breakdown

Buffer, between isolated ohmics
5µm separation

Transistor, L_g = 120nm

Courtesy of: F. Medjdoub/IEMN, on EpiGaN material

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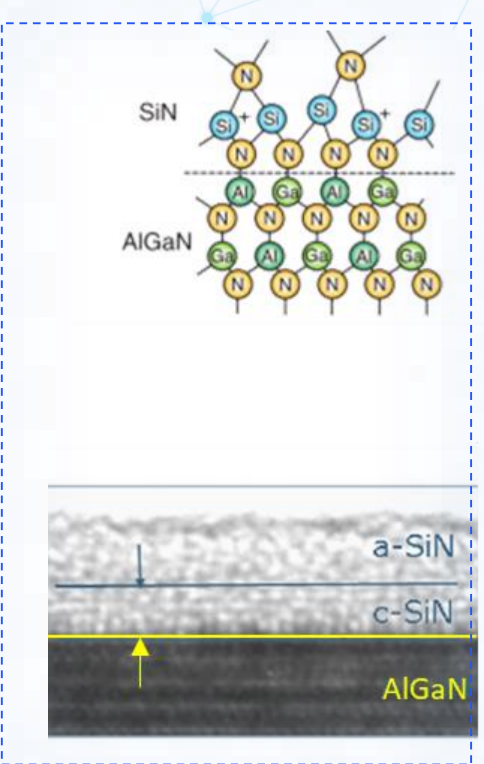
In-situ SiN – more than surface passivation

- 'Very early' and efficient passivation approach
- High-density SiN
- High-quality gate dielectric
- Higher n_s and mobility compared to GaN cap
- Prevents relaxation of (Al,Ga)N barrier
- Improved thermal stability, device reliability
- Reduces contamination risks in CMOS fabs



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Tuning the heterostructure for the required RF/mm-wave performance

- **Reference structure today mostly use AlGaN/GaN heterostructures with either SiN or GaN cap** ***(reference structure today used in 3G/4G <sub6Ghz & X Band)***

  Typical electrical specifications:

  - μ > 1800 cm2/V.s for $n_S \sim 1\ e^{13}/cm^2$ with SiN cap
  - Offers Low leakage for Schottky and (SiN) MIS-HEMTs

- **BUT mm-wave requires more advanced type of heterostructures**

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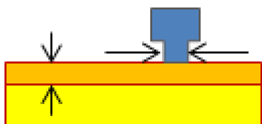
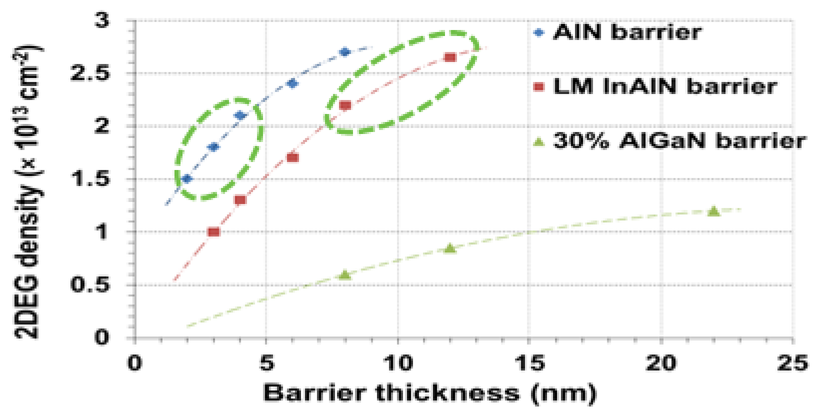
mmwave operation : possible strategies

- Heterostructures for maximal g_m
  - Gate-to-channel aspect ratio
    - Ultrathin AlN
  - Maximise I_{ds} => Reduction of R_{sheet}
    - InAlN with R_{sheet} < 250 Ohm/sq.

$$f_t \approx \frac{g_m}{2 \cdot \pi \cdot (C_{gs} + C_{gd})}$$



$$g_m = \frac{dI_{ds}}{dV_g}$$



Strain imposes different thickness regimes

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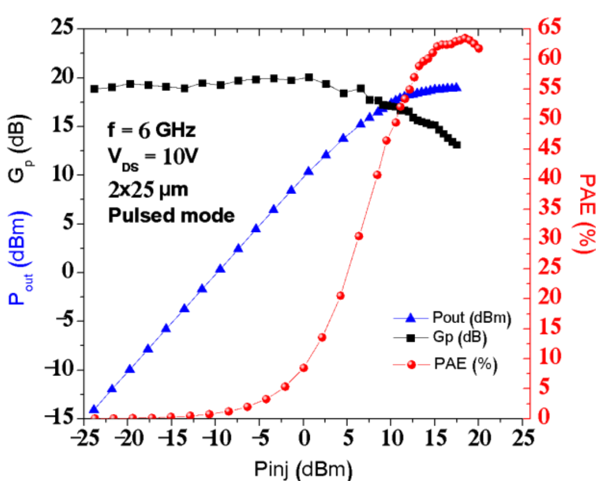
HVRF SiN/AlN HEMT on Si @6GHz

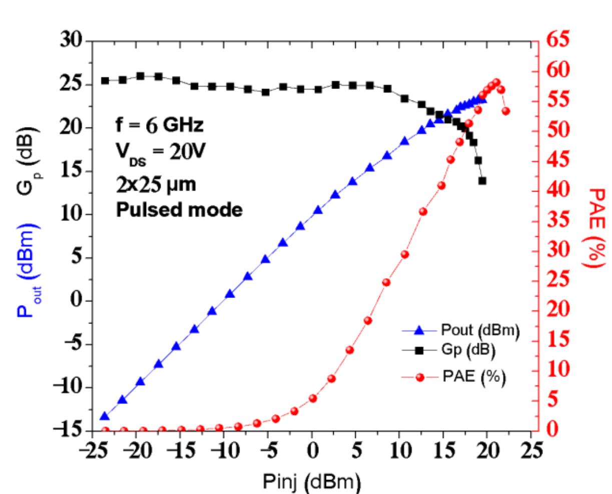
V_{DS} = 10 V

Saturated P_{OUT} = 1.6 W/mm



V_{DS} = 20 V

Saturated P_{OUT} = 4.2 W/mm



Courtesy of: F. Medjdoub/IEMN;

T-Gate: 150nm, no wafer thinning nor TSV, Deep class AB, I_D = 100mA/mm

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InAlN carrier density mobility optimization

Sheet resistance versus 2DEG density

Rsheet [Ohm/sq.] vs ns [1/cm2]

Electron Mobility vs. 2DEG density

Mobility [cm2/V.s] vs ns [1/cm2]

- **Excellent 2DEG transport properties:**
  - ✓ Hall: n_s between $1.3\times10^{13}/cm^2$ and $3.2\times10^{13}/cm^2$ (depending on barrier thickness and composition)
  - ✓ R_s = 170 Ohm/sq (μ= 1,800 $cm^2/V.s$ @ ns = $1.6\times10^{13}/cm^2$

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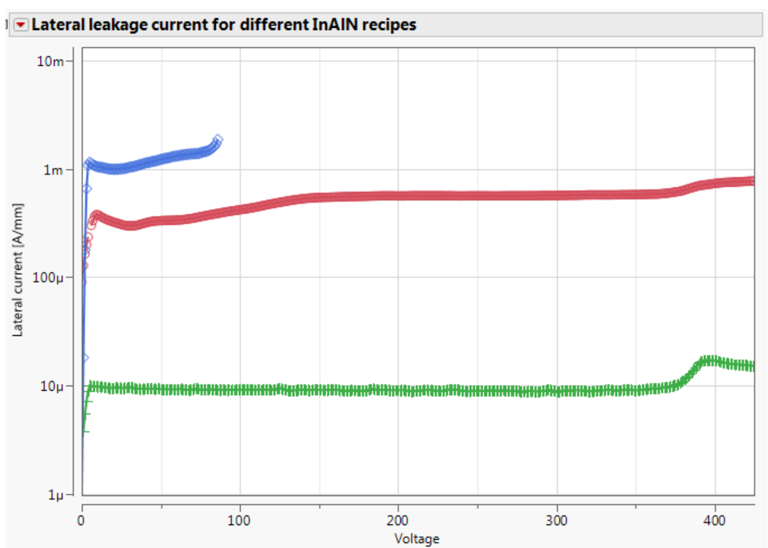
Leakage current reduction with InAlN barriers

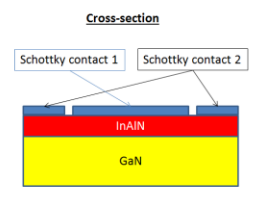
- MOCVD process tuning allows for
  - Leakage current reduction (down to 10µA/mm)
  - Lateral breakdown voltage increase (buffer limit)

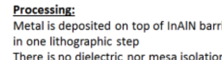


Measured between two concentric Ni/Au Schottky contacts in direct contact with InAlN barrier, with spacing 14µm

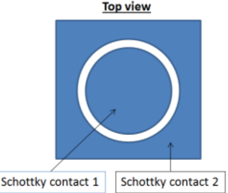
Normalised to periphery [A/mm]

Cross-section





Top view



Diameter center contact = 150 µm
=> Periphery = 471µm
Spacing = 4, 12 or 32µm

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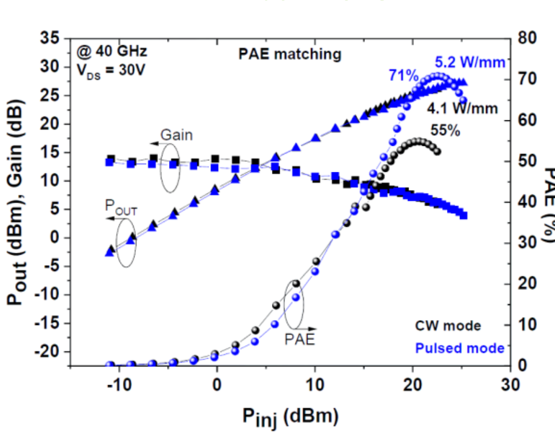
mmWave performance of Soitec epitaxial wafers

Active load-pull on 2x50um transistors with Lg = 110nm

AlN barriers

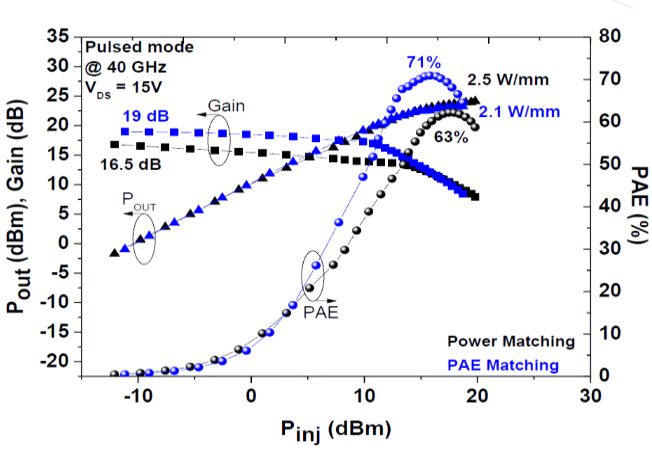


Robust HEMT
Operating at 30V

SotA power density and PAE

Gain, Ft, fmax limited by electron mobility

InAlN barriers



SotA PAE and good power density

High gain due to much larger ft / fmax

Robustness is a critical point of attention

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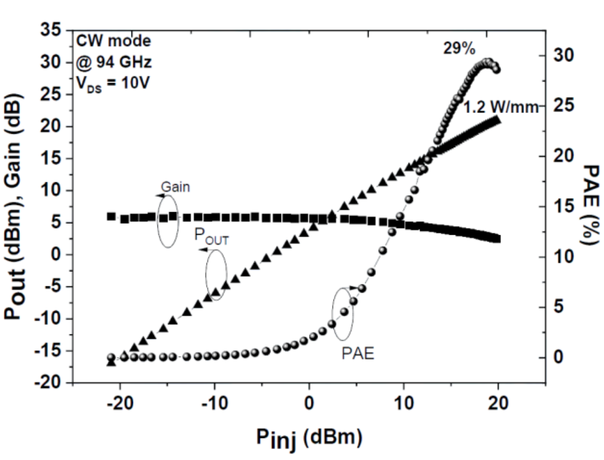
Courtesy of: F. Medjdoub/IEMN

W-band performance of Soitec epitaxial wafers

Active load-pull on 2x25um transistors with Lg = 80nm

AlN barrier



SotA power density and PAE for 94GHz

Gain is rather low (due to ft/fmax)

The performance of InAlN barriers with very short gate lengths (<< 100nm) needs to be explored to achieve high gain, PAE and power density at the same time.

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Take-Aways

- GaN-on-Si technology up to 200mm (next 300mm) epiwafers products enables most cost-efficient GaN technology deployment for volume by leveraging from Si fab manufacturing

- In-situ SiN capping offers not only optimal surface passivation but also enables ultimate performance barriers and is compatible with ohmic contact regrowth.

- Latest EpiGaN-RF product family developments with SiN/(In,Al)N top structures are a key enabler for sub-6GHz and mmW NR 5G applications

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