D5.5

Fabricated and tested module

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Abstract:	In the course of the SERENA project research on the design and manufacturing of an antenna-in-package module containing a GaN amplifier IC and a SiGe beam forming IC for 5G mmWave applications was performed. The module uses a low-cost packaging technology. The report contains details on the design, manufacturing process and the characterization of the modules.
Keywords:	5G, mmWave packaging, Antenna-in-Package

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Executive Summary

During the SERENA project an antenna-in-package packaging technology for mmWave front-ends has been developed. The packaging technology is based on a PCB embedding technology and supports the heterogeneous integration of mmWave ICs and an antenna array. The packaging technology allows for very short RF interconnects with controllable characteristic impedance. The antenna-in-package modules are compatible to PCB solder.

For the development of the SERENA demonstrator based on the packaging technology two modules were developed: a low-power module containing the SiGe beam forming IC from Infineon and the high power version containing in addition the GaN power amplifier IC from OMMIC.

Based on measurements of the RF characteristics before and after embedding (packaging) the ICs the impact of the package was estimated. The functionality of the fabricated low-power modules was tested based on the assessment of the SPI communication.

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Chapter 1 Introduction

In the project SERENA, research on electronics hardware for 5G mmWave base stations is performed. There are a number of mmWave frequency bands used for 5G applications, including the 39 GHz band. At mmWave frequencies (> 30 GHz) attenuation due to free space loss and the atmosphere introduce strong signal loss and is thus limiting the transmission distance. To overcome the losses it is important to minimize the signal loss at mmWave in the system. The antenna-in-package concept allows for a tight integration of the components for RF signal generation and the antenna.

In the course of SERENA an advanced PCB embedding technology was developed to realize antenna-in-package modules for mmWave applications (cf. [1], [2] and [3] for details). The module allows heterogeneous integration of five ICs (a SiGe beam former IC, four GaN power amplifiers) and additional chip capacitors. The embedding technology also allows to place the ICs inside the package and create very short electrical interconnects to the antenna array that is integrated at the top surface of the package. In addition the modules have dense thermal vias on the bottom for efficient thermal path.

The deliverable presents the design of the modules and provides details on the manufacturing and the results of the electrical characterization based on RF measurements.

This document is organized as follows

- Followed by introduction is the overview of the SERENA modules which includes design aspects of low power and high power modules in Chapter 2
- The fabrication of the modules is discussed in Chapter 3
- The measurement procedure and corresponding results of the fabricated modules are presented in Chapter 4
- In the end Chapter 5 concludes the document

Chapter 2 Overview of SERENA Modules

The system comprises of the front-end components for RF signal amplification and phase shifting, a frequency converter, an antenna array and the MIMO SDR system by partner TU Berlin. The Serena module integrates the components for RF amplification and phase control as well as the antenna array. Figure 1 shows the block level diagram of the Serena demonstrator.

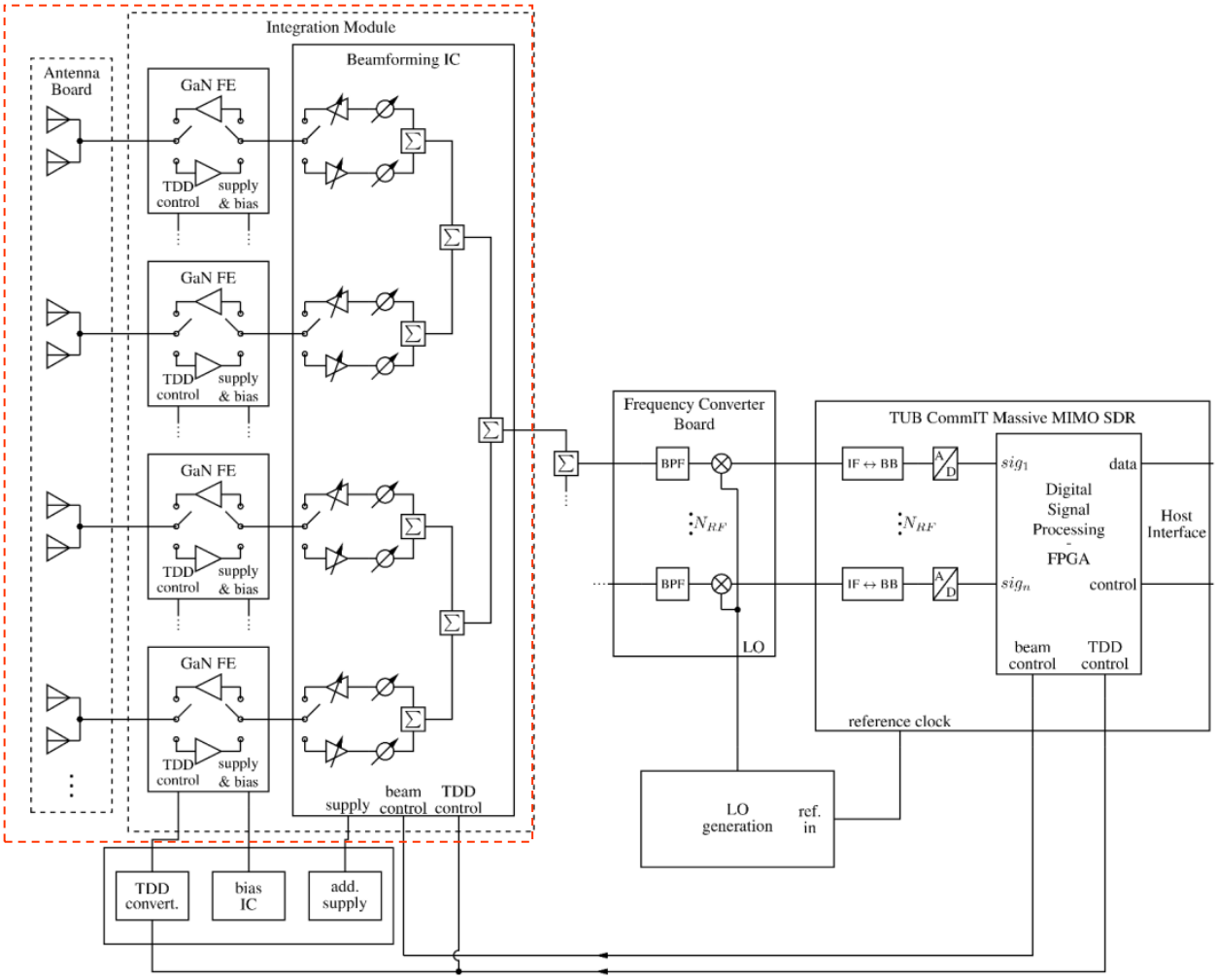


Figure 1 Block level diagram of Serena demonstrator with front-end package (inside red dashed line) [4]

The block level diagram of the SERENA module shows the individual functional blocks. The RF signal processing is divided between two ICs:

- a four channel beamforming IC with controllable phase shift and medium power amplifier per channel and
- a single channel Tx/Rx power amplifier IC.

In order to be able to evaluate the individual ICs contained in the package two versions of the SERENA module were planned: a low power module containing the beam-former IC and a high power module containing both the beam former and power amplifier ICs.

Both modules are designed to have the identical LGA footprint and semi-identical pin map thus enabling the usage of the same system board for both the modules. They are identical in size

(9.5 x 15 mm^2) and compatible in their electrical pin designations. Both module variations allow the Tx/Rx operation of the module for the project demonstration. The additional power amplifier IC in the high power module allows for higher transmission range.

The design of both the modules will be discussed in the following section

2.1 Low-power Serena Module

The low-power module consists of the 39 GHz beamformer IC from Infineon integrated along with an antenna array [yellow] (Figure 2). In addition 100 pF decoupling capacitors for each V_{DD} voltage supply pin are included for power integrity in the low-power modules.

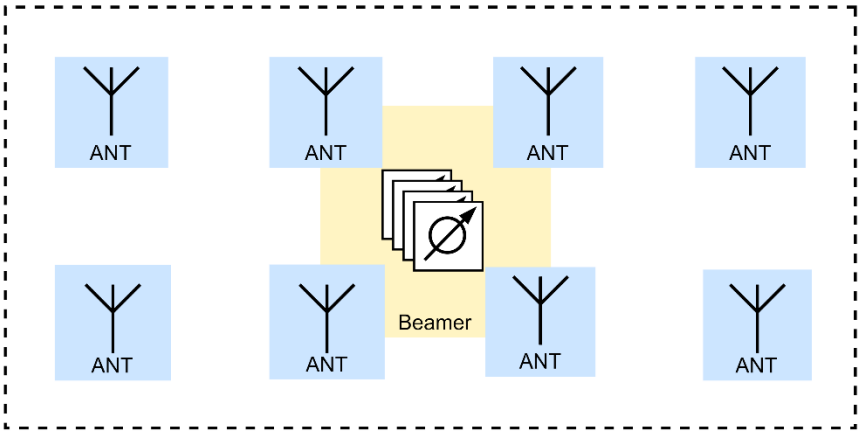


Figure 2 Schematic view of low power module indicating the placement of the beamer IC and the antennas

The LGA footprint and the pin-map for the low-power module was finalized in collaboration with Ericsson (Figure 3). The footprint and pin-map of both high power and low power modules were harmonized to be compatible with each other and the system board. The harmonization is enabled by having an open connection in the systemboard level for the specified pins in the low power module. The specified pins are based on the functionalized pins in the high power module. This is because of the larger number of pin requirements that arises with the embedding of additional 4 PA ICs in the high power modules.

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	
1	GND	GND	GND	GND	GND	GND	GND	GND	open	open	open	GND	open	GND			1
2	GND	open													GND	GND	2
3	GND	open													open	open	3
4	GND	GND													GND	GND	4
5	GND	GND						Thermal Pad/ GND							GND	open	5
6	open	GND													GND	open	6
7	open	GND													GND	GND	7
8	open	open			GND	open	VDD_PLL	REFCLK_N	REFCLK_P	VDD_P	open	GND			open	open	8
9	open	VDD_PA1	GND	GND									open	open	VDD_PA2	open	9
10	open	VDD_P	GND	GND									GND	GND	VDD_P	open	10
11	GND	GND	GND	VDD_P									VDD_P	GND	GND	GND	11
12	GND	GND	GND										SDO	GND	GND	GND	12
13	RFIO							Thermal Pad/ GND					TXRX_I	GND	GND	GND	13
14	GND	GND	GND										CSN	DCLK_I	GND	GND	14
15													SDI	open	GND	GND	15
16	open	VDD_P	GND	GND									GND	GND	VDD_P	open	16
17	open	VDD_PA4													VDD_PA3	open	17
18	open	open	GND	GND	GND	GND	VDD_P	open	GND	VDD_P	open	open	GND	GND	open	open	18
19	GND	open													GND	GND	19
20	GND	open													open	open	20
21	GND	GND						Thermal Pad/ GND							GND	GND	21
22	GND	GND													GND	open	22
23	open	open													open	GND	23
24	GND	GND													GND	GND	24
25	GND	GND	GND	GND	open	open	open	open	GND	GND	GND	GND	GND	GND	GND	GND	25
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	

Figure 3 LGA pin-map of the low-power module

The embedded module has six metal layers as shown in Figure 4 with metal layers L2 and L3 for signal and supply redistribution and a keepout region above the IC. Megtron7N PCB material by Panasonic is used as the dielectric material for PCB based embedding modules, while on top of the IC a thin Ajinomoto ABF dielectric layer is used. The “Top” layer is the antenna layer whereas, metal layer L1 is used as the antenna ground. Thermal vias between L4 and the bottom layer are used to connect the ICs to the bottom LGA interface, acting as a thermal path for the heat generated in the ICs through the LGA layer to the systemboard.

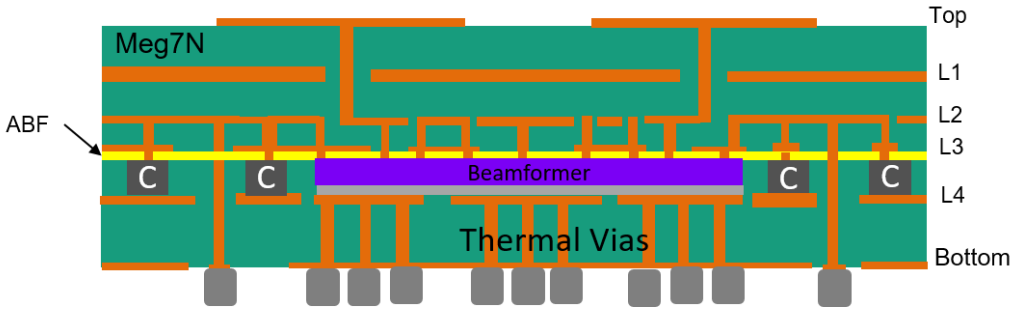


Figure 4 Cross section of the module material stack-up of the low-power module [5]

The RF signal paths inside the module from the beamformer IC to systemboard and antennas (cf. black lines in figure 5) were designed to have low insertion loss and return loss using EM field simulations using Ansys HFSS.

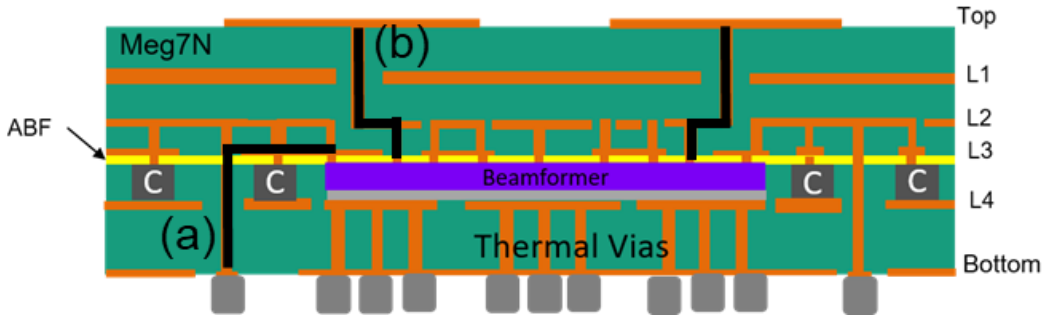


Figure 5 Signal path (a) System board to the IC (b) IC to the antenna [5]

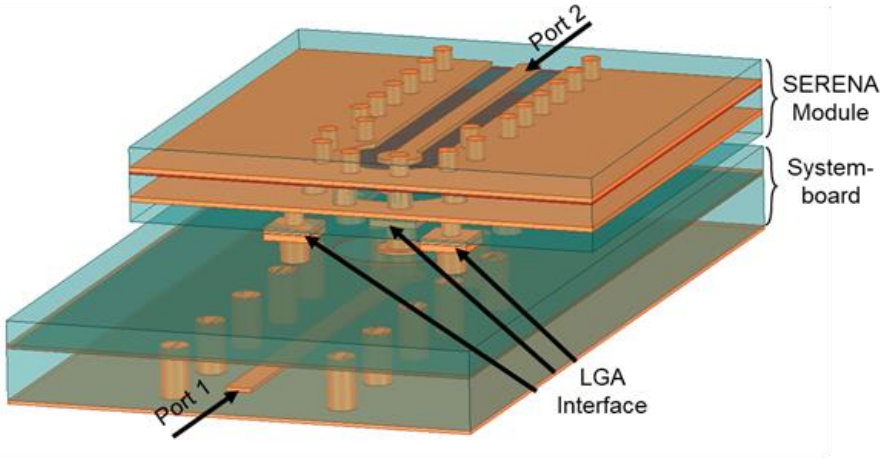


Figure 6 Simulated signal path model from system board to the IC

In order to provide good impedance matching to the beam former IC the signal trace of the strip line in the system board were optimized to 50 Ohm characteristic impedance at 137 µm signal trace width and the slot width of the grounded coplanar waveguide is 110 µm and 150 µm respectively and connected by LGA interface as shown in the Figure 6. The simulated S-parameters are shown in Figure 7 with return loss below 25 dB and insertion loss below 0.4 dB

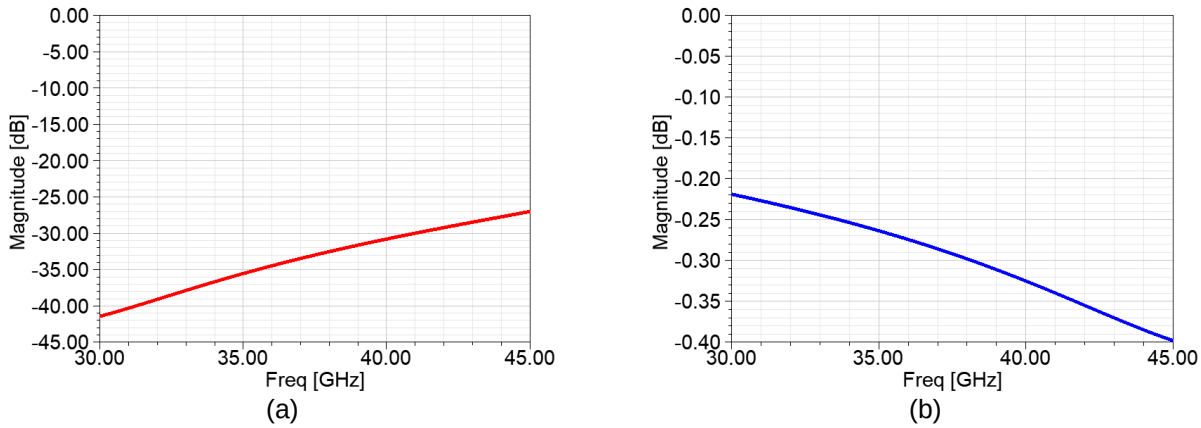


Figure 7 Simulated signal path from system board to the IC (a) return loss (b) insertion loss

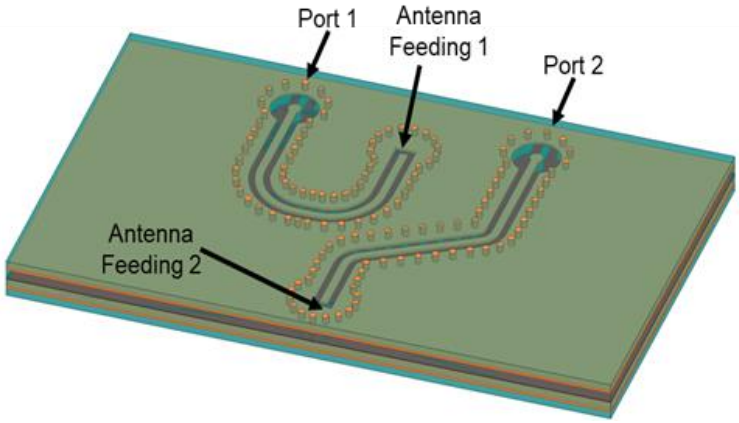
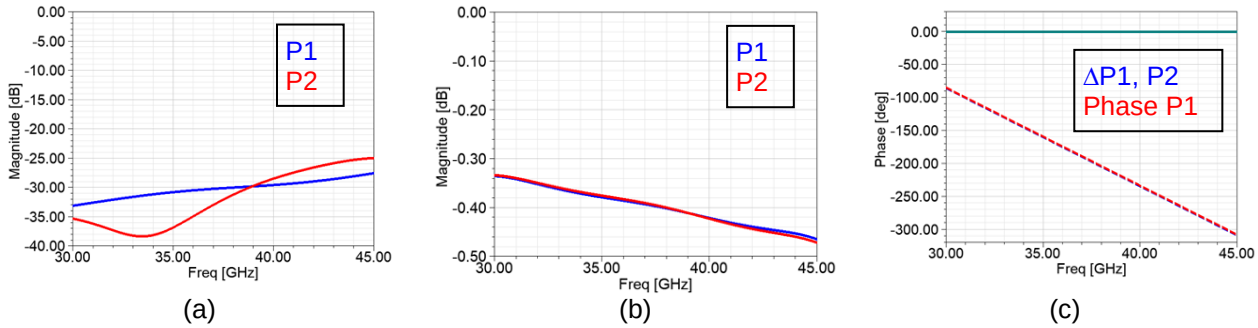


Figure 8 Simulated signal path model from IC to Antenna. P1: Port 1-Antenna, P2: Port2-Antenna

The signal path from the beamformer IC to the antenna were optimized to have low loss as well as low phase difference between two different paths. The simulated signal path is as shown in the Figure 8. A grounded co-planar waveguide (GCPW) is used as the transmission line for the feeding of the antenna along with two via transitions. The length of both the signal paths was designed to have a total length of approximately 6 mm. The performance of the simulated signal path is as shown in the Figure 9. The trace width and slot width of L4 GCPW are 123 µm and 100 µm respectively and 110 µm and 150 µm for the L3 GCPW layer. The simulated results show that the return loss is below 25 dB, the insertion loss is below 0.5 dB and the phase difference achieved was 0.79 ° at 40 GHz which is within the limits of beamformer IC (less than 5 deg).



(a) (b) (c)

Figure 9 Simulated signal paths from IC to Antenna (a) Return loss (b) Insertion loss (c) Phase difference.

The antennas along with the signal path were simulated to cover the whole band as shown in Figure 10.

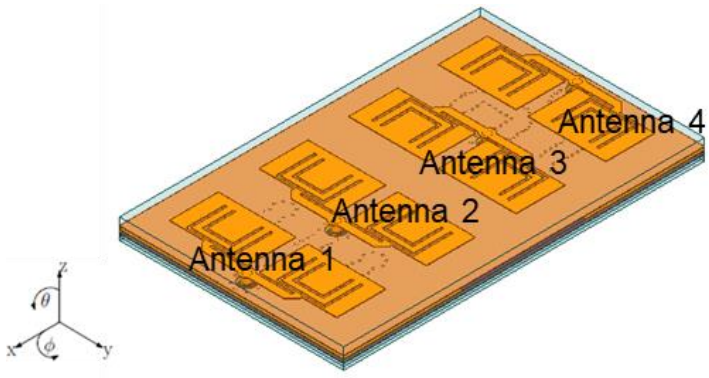


Figure 10 3D – View of simulated antenna including signal path

The bandwidth of the antennas 1 and 4 is 4 GHz (37.3-41.3 GHz) and for antennas 2 and 3 is 4.5 GHz (37.1-41.6 GHz). The realized gain of the full array is 13.5 dBi @ 38.5 GHz (Figure 11).

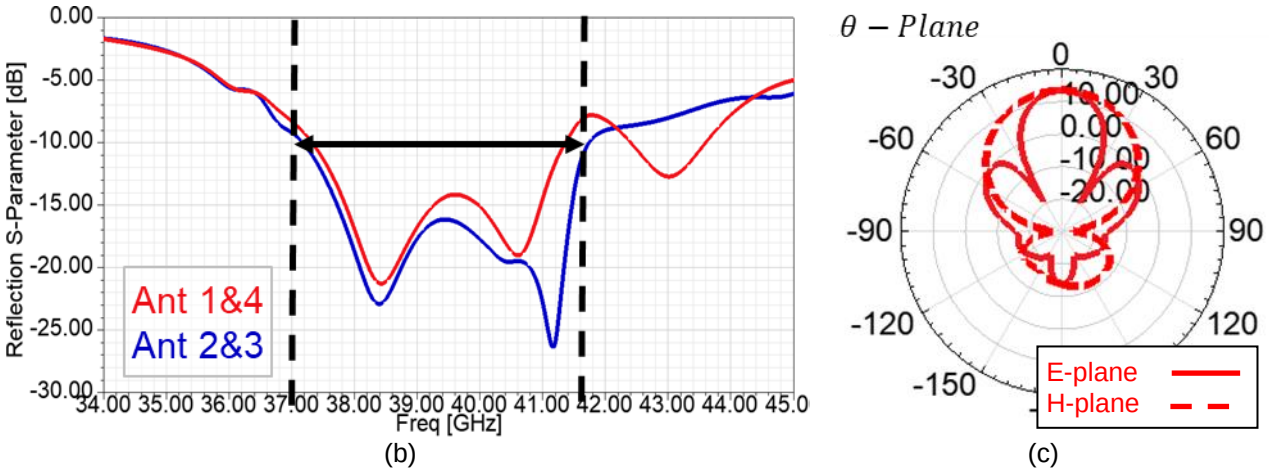


Figure 11 Simulated antenna including signal path (a) Reflection S-pararmeters (b) 2D - radiation pattern

2.2 High-power beamformer module

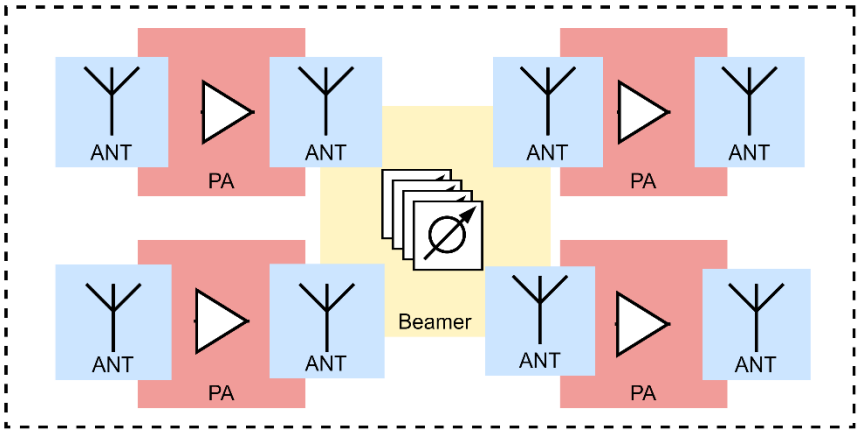


Figure 12 Schematic of high power module

The high power module consists of beam former as well as the power amplifiers along with the antenna array. As mentioned in the low power module the pin map of the high-power module is compatible to the low power module, as shown in the Figure 13. As mentioned earlier, the open pins in the low power model corresponds to the power amplifier pins in high power module. The high power module has the same substrate stack-up as the low power module.

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	
1	GND	GND	GND	GND	GND	GND	GND	GND	O4_VD	O4_SW1	O3_SW3	GND	O3_VS_LNA	GND			1
2	GND	O4_VG													GND	GND	2
3	GND	O4_SW2													O3_SW4	O3_VD_LNA	3
4	GND	GND													GND	GND	4
5	GND	GND						Thermal Pad/ GND							GND	O3_SW2	5
6	O4_SW4	GND													GND	O3_VG	6
7	O4_VD_LNA	GND													GND	GND	7
8	GND	GND			GND	O4_VS_LNA	VDD_PLL	REFCLK_N	REFCLK_P	VDD_P	O4_SW3	GND			GND	GND	8
9	GND	VDD_PA1	GND	GND									O3_SW1	O3_VD	VDD_PA2	GND	9
10	GND	VDD_P	GND	GND									GND	GND	VDD_P	GND	10
11	GND	GND	GND	VDD_P									VDD_P	GND	GND	GND	11
12	GND	GND	GND										SDO	GND	GND	GND	12
13	RFIO							Thermal Pad/ GND					TXRX_I	GND	GND	GND	13
14	GND	GND	GND										CSN	DCLK_I	GND	GND	14
15													SDI	DCLK_O	GND	GND	15
16	GND	VDD_P	GND	GND									GND	GND	VDD_P	GND	16
17	GND	VDD_PA4													VDD_PA3	GND	17
18	GND	O2_VD	GND	GND	GND	GND	VDD_P	O2_SW1	GND	VDD_P	O1_SW3	O1_VS_LNA	GND	GND	GND	GND	18
19	GND	O2_VG													GND	GND	19
20	GND	O2_SW2													O1_SW4	O1_VD_LNA	20
21	GND	GND						Thermal Pad/ GND							GND	GND	21
22	GND	GND													GND	O1_VG	22
23	O2_VD_LNA	O2_SW4													O1_SW2	GND	23
24	GND	GND													GND	GND	24
25	GND	GND	GND	GND	O2_VS_LNA	O2_SW3	O1_SW1	O1_VD	GND	GND	GND	GND	GND	GND	GND	GND	25
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	

Figure 13 Pin map of high power module

The signal path from system board to the IC is same as for the low power module while the signal paths from chip to the antenna is different for the high power modules as the antenna is fed from the OMMIC IC instead of the Infineon IC as in low power module. The simulated signal paths of high power modules are shown in Figure 14.

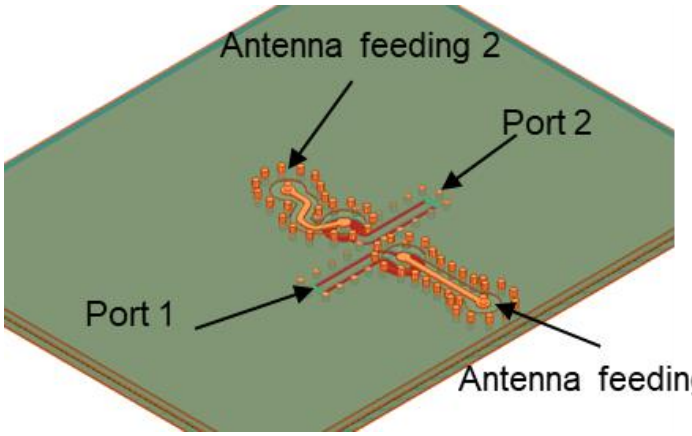


Figure 14 Simulated signal path model from IC to Antenna. P1: Port1-Antenna feeding1, P2: Port2-Antenna feeding2

The signal path from power amplifier IC to the antenna are designed to have low loss as well as to have minimum phase difference between two different paths. The simulated signal path is as shown in the Figure 14. A grounded co-planar waveguide (GCPW) is used as the transmission line for the feeding of the antenna along with two via transitions. The length of both signal paths was designed to have a total length of approximately 2.2 mm. The performance of the simulated signal path is as shown in the Figure 15. The trace width and slot width of L4 GCPW are 95 µm and 100 µm respectively and 100 µm and 90 µm for the L3 GCPW layer. The simulated results show that the return loss is below 30 dB, the insertion loss below 0.3 dB and the phase difference achieved was 0.2° at 40 GHz which is within the limits of beamformer IC (5°). The losses and phase difference of

signal paths are lower than that of the low power module as the signal path is shorter and closer to the antenna feed point.

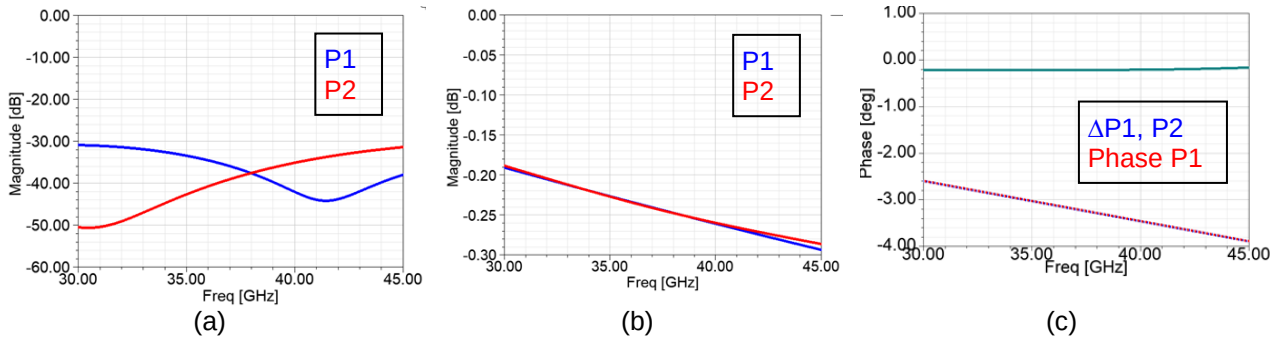


Figure 15 Simulated signal path from power amplifier IC to Antenna (a) Return loss (b) Insertion loss (c) Phase difference

Antennas were designed and simulated including the signal paths to cover the whole band after including the signal paths. The bandwidth of the antennas 1 and 4 is 4.32 GHz (36.97-41.29 GHz) and for antennas 2 and 3 is 4.63 GHz (37.17–41.36 GHz). The realized gain of the full array is 13.6 dBi @ 39 GHz.

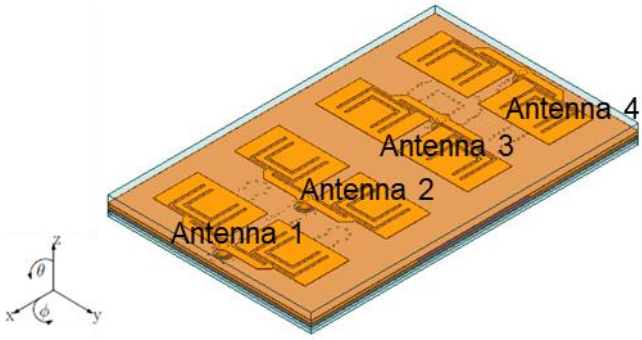


Figure 16 3D-view of simulated Antenna including signal path

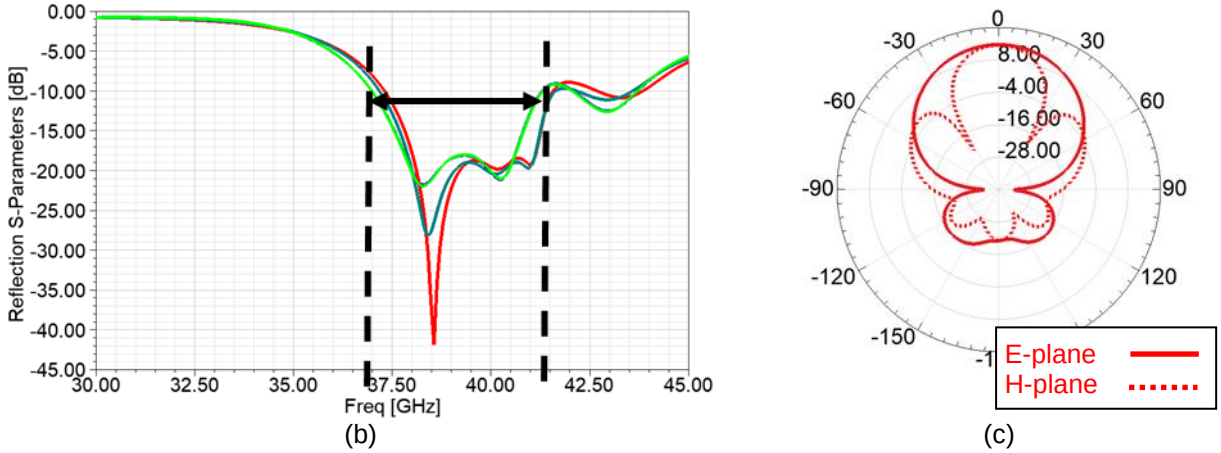


Figure 17 Simulated antenna including signal path (a) Reflection S-pararmeters (b) 2D - radiation pattern

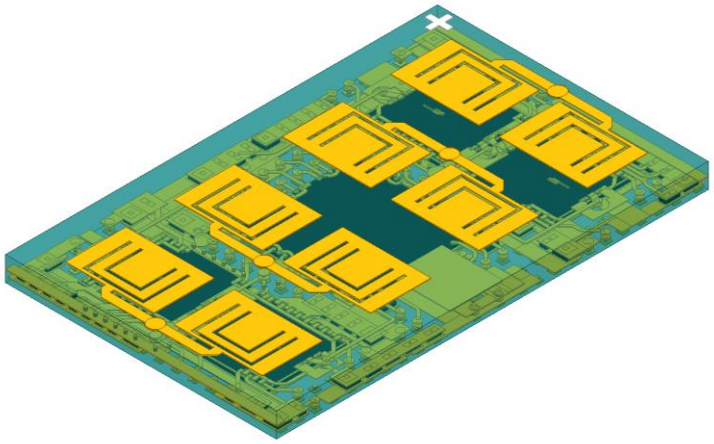


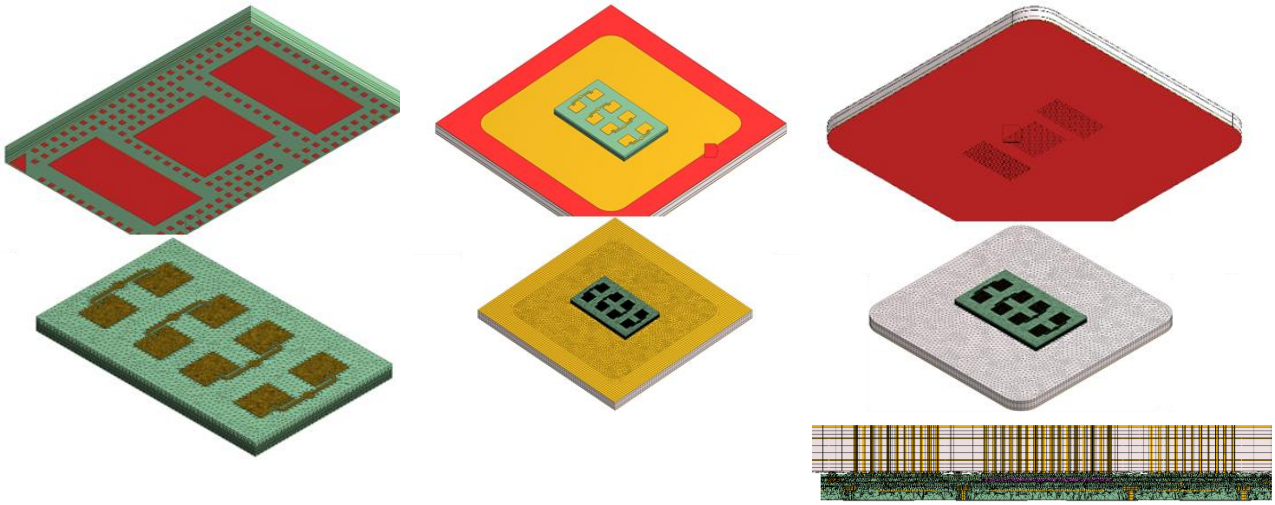
Figure 18 3D – View of the high power module

Figure 18 shows a CAD rendering of the higly integrated high power module.

2.3 Thermal transient simulation

Thermal transient simulations were performed based on the design of the full power module with three different test boards

- Case 1: Without any test board
- Case 2: With test board according to JEDEC specification
- Case 3: With test board – specified by Ericsson



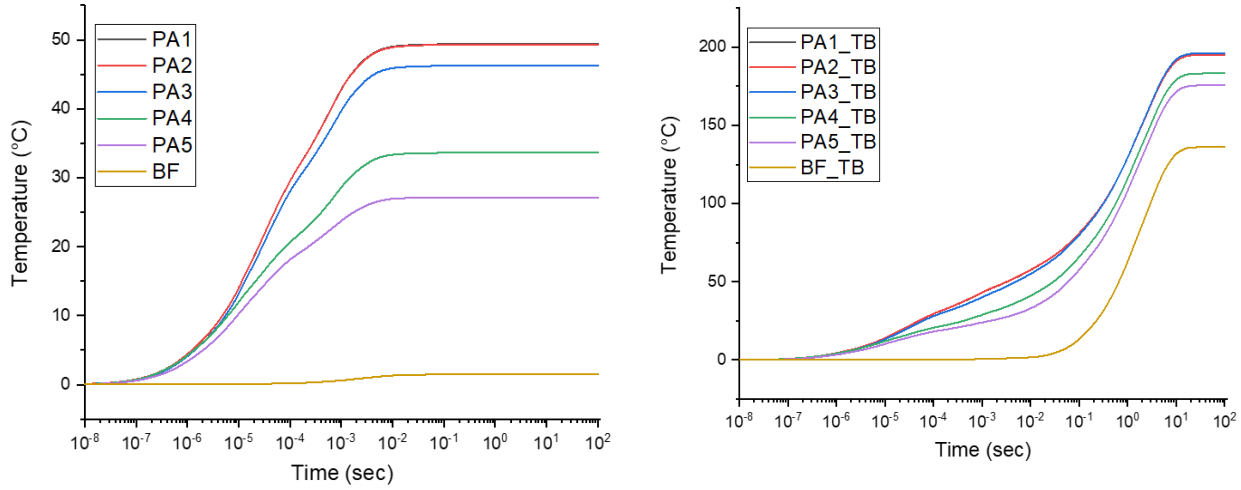
(a) (b) (c)

Figure 19 Transient simulation test boards temperatures (a) case 1 (b) case 2 (c) case 3

In case 1 no test board is used at the bottom of the embedding module and the bottom is kept at constant temperature of 0 °C. In case 2, a test board based on JEDEC standard JESD51-9 is attached to the bottom of the module with a ring around the test board and the bottom of the test board fixed at 0 °C. In case 3, a test board specified by Ericsson with filled thermal vias inside the test board with 0 °C and 22 °C boundary conditions at the bottom of the test board were used. Logarithmic time steps were used for transient simulations with the first time step ending after 100 ns.

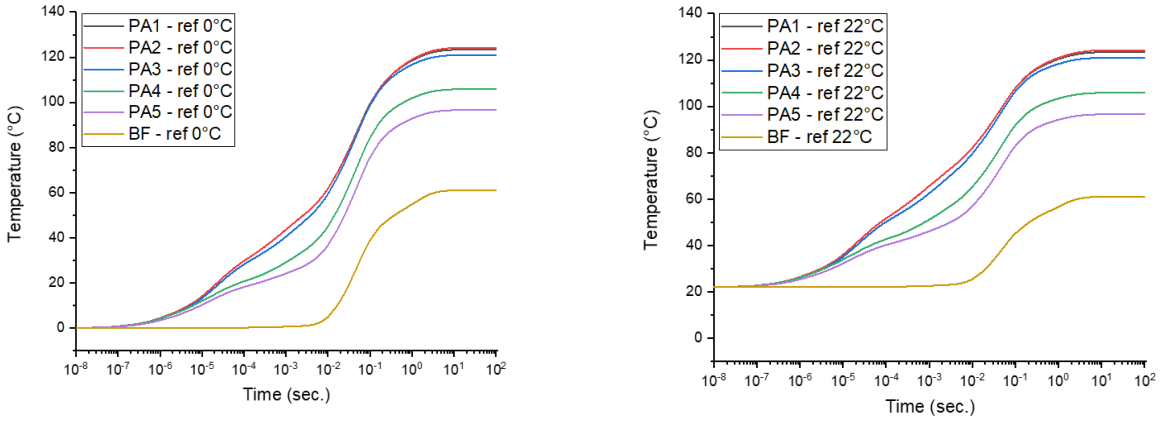
The simulations were done for different positions in the module, PA1-PA5 corresponding to the thermal hot spots on the OMMIC power amplifier IC and BF to a location on the Infineon Beam forming IC.

The results for thermal transient simulation are as shown below, showing that the case 1 with low thermal resistance path has lower final temperature than case 2 and case 3. In case 3 with Ericsson test board two different starting temperatures (0°C and 22 °C) were used, without any noticeable change in transient thermal performance.



(a) (b)

Figure 20 Transient simulation results (a) case 1 (b) case 2



(a) (b)

Figure 21 Transient simulation results (a) case 3 – 0 °C starting temperature (b) case 3 - 22 °C starting temperature

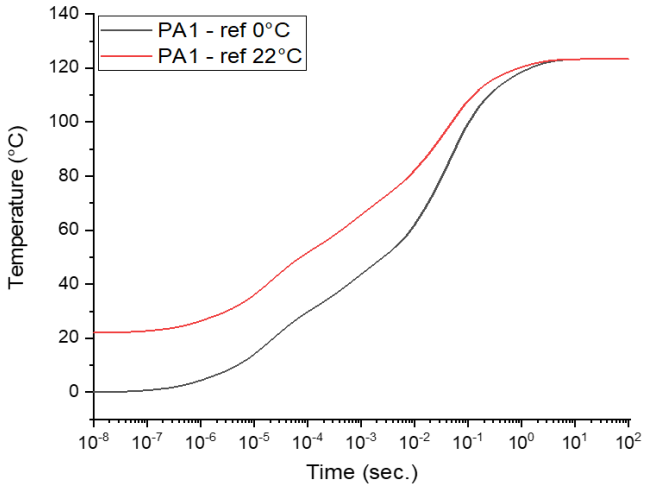


Figure 22 Transient simulation comparison case 3 – (0 °C & 22 °C)

Chapter 3 Fabrication of Modules

The fabrication of the low power module involves advanced PCB embedding of heterogeneous components. In low power module the embedding involves the beamformer IC along with 100pF decoupling capacitors, and multiple stacked vias. In total, the fabrication of low power module has more than 130 process steps.

3.1 Process Flow

The designed module is fabricated at using IZM's PCB embedding technology. The PCB embedding consists of two main steps (Figure 23)

1. Embedding
2. Sequential lamination

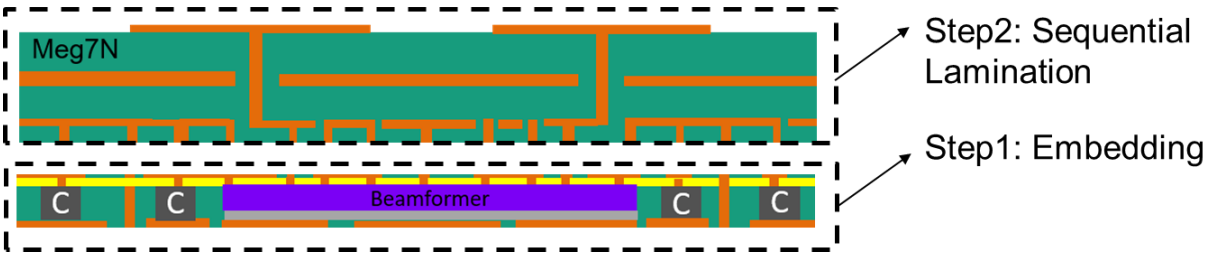


Figure 23 Steps for fabrication of embedding module

The embedding process of IC and other components (capacitors) involves

1. Component placement: Assembly of the ICs and capacitors on the PCB substrate using sinter glue.
2. Embedding: Using an ABF dielectric layer and laser structured Megtron 7N prepreg the ICs and capacitors are embedded inside the PCB modules.
3. Electrical connections: Laser drilling (Figure 24, a) followed by sputtering process (Figure 24, b) and special electroplating to achieve levelled via filling (Figure 24 c) is used for establishing electrical connection with the components.

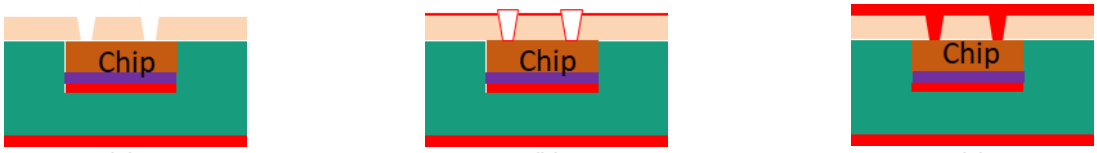


Figure 24 Steps for embedding of components

The embedding is followed sequential processes of lamination, laser drilling, metallization, structuring and pre-treatment for the next lamination steps.

3.2 Fabricated Modules

3.2.1 Assembly test

To ensure the correct functionality critical process steps were identified and the developed processes validated. Two critical manufacturing steps were identified. The first one is the pick-and-place of the IC onto the PCB core in combination with a silver sinter process. The second citical step is the embedding of the IC.

In order to validate the assembly test structures for the placement of capacitors were performed to verify the fabrication capability of the design. Highest complexity in the proximity of the components (capacitors) is identified from high power module to ensure the assembly process of embedding modules. Figure 25 show realized test assemblies with capacitors on a test substrate. The pictures verify the necessary placement accuracy of the pick-and-place operation at very low proximity between components.

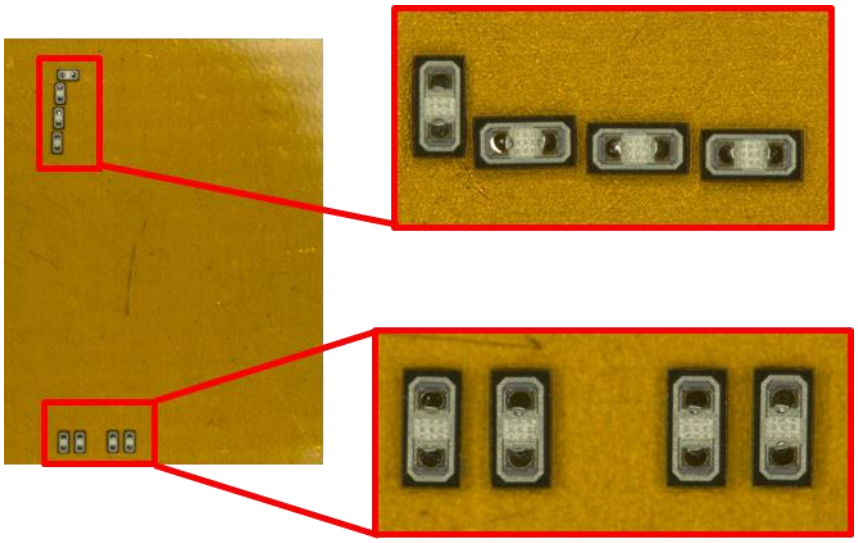


Figure 25 Microscopic picture of assembly test for the capacitors in SERENA module

3.2.2 Low-power module

The fabrication process step involves microscopic examination after each and every process step. Figure 26 shows the fabricated vias connecting the dies inside the package and the different metal layers in the package. The top row shows the vias to the die after laser drilling and, the bottom left pictures shows the metal traces connecting the IC though the vias. The positioning of the via shows only low tolerances due to the fabrication process.

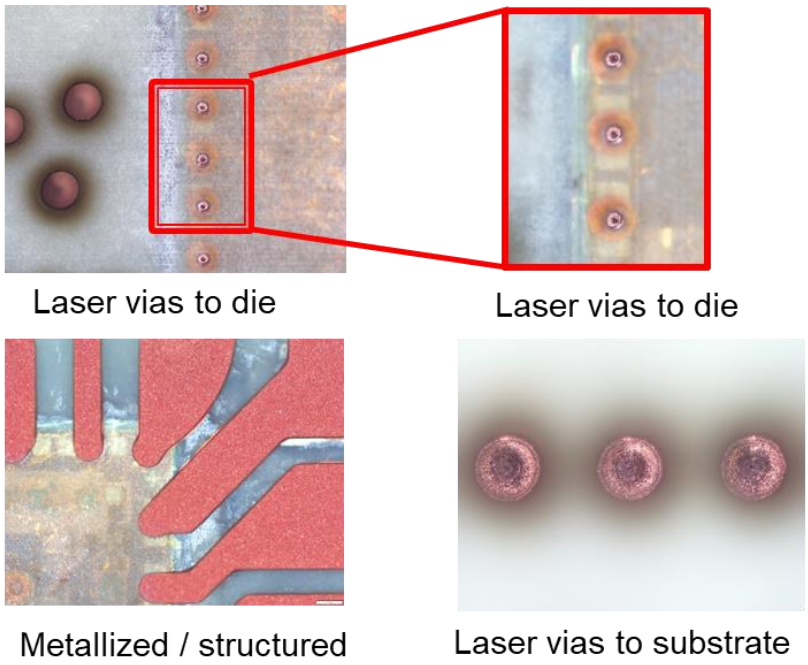


Figure 26 Laser through ABF film to IC pads

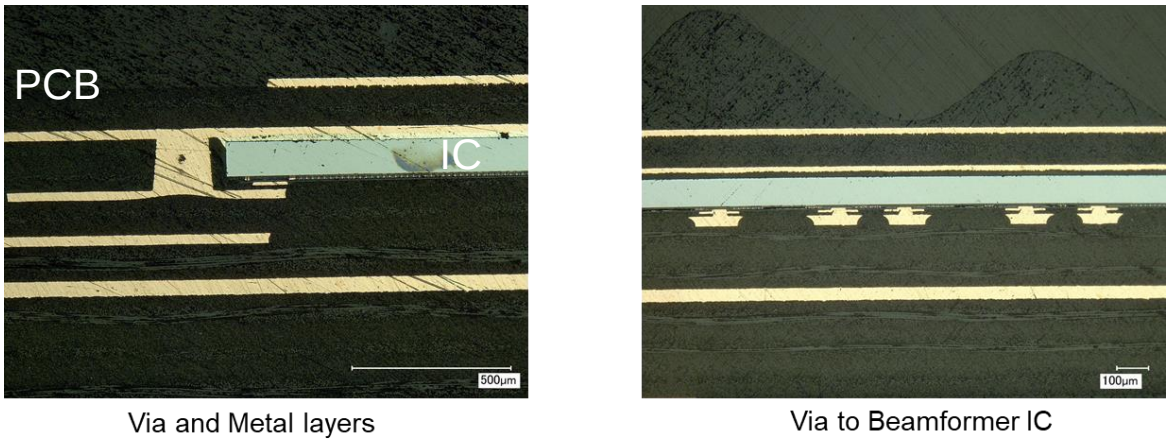


Figure 27 cross-sectional view (chip active side is looking down)

Figure 27 shows cross sections of one of the packages. On the left the IC is mounted using Ag sinter glue on its backside to the underlying metal layer for good heat dissipation. The filled via next to the IC shows good planarity with only a minor topography over the via. The picture on the right shows stacked vias from the die to inside the package. The cross sections show good alignment between stacked vias and pads.

In addition to the microscopic investigation, X-ray imaging were used to see through the dielectric layer to review the alignment of the stacked vias, planar signal path interconnects as well as vias to the IC connection. Figure 28 shows X-ray images of the fabricated low-power modules. On the left of Figure 28 one can see the beam forming IC in the center and the four RF antenna feeding lines connecting to the ICs. In addition the high number of vias required to ensure the EMI of the module. The low power module contains approximately 2700 microvias.

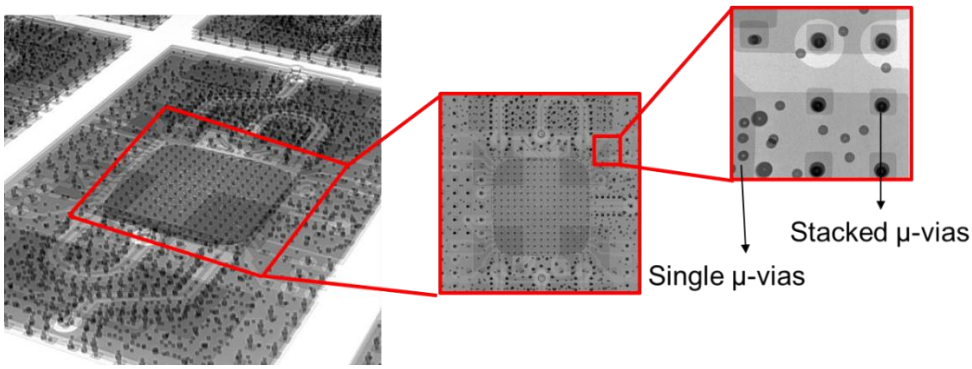


Figure 28 X- ray image of fabricated low-power modules

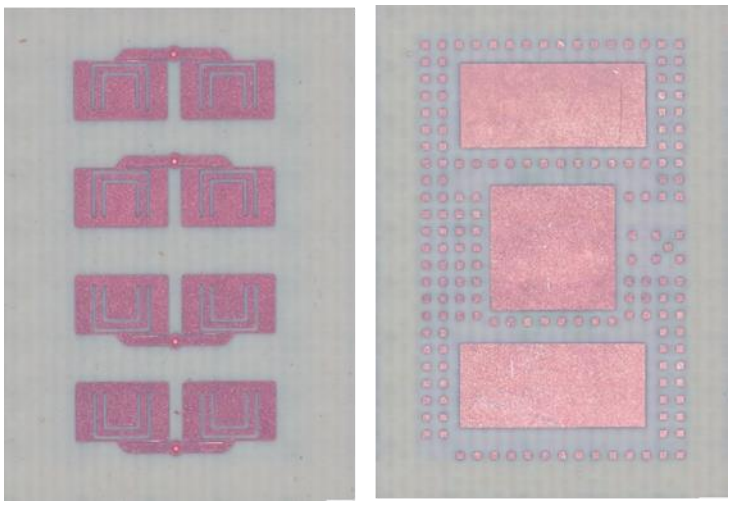


Figure 29 Top (left) and bottom (right) layer side of the package

Figure 29 shows photographs of the top side with the antennas and the bottom side with the IO pins and the thermal pads of the package.

The investigation show that the fabricated modules are showing low tolerances and highly accurate fabrication.

Chapter 4 Measurement

4.1 GaN Amplifier IC

In order to characterize the impact of the embedding on the electrical performance of the GaN amplifier ICs, electrical characterization after each step was followed. This involves the measurement of bare die delivered by OMMIC at Fraunhofer IZM followed by measurement after assembly, and finally by measurement after embedding and metallization steps.

4.1.1 Measurement Set-Up

These measurements were carried out on a manual wafer probing system (Cascade Microtech, model Summit 11000), using RF GSG probes for the high frequency contact pads (Cascade Microtech, MPI). For the bare-die measurements for reference purposes, DC needles provided the supply voltages, see Figure 31, whereas in the post-embedding measurement, standard pin header SMD connectors were directly soldered onto to samples, as shown in Figure 33. In this setup, the S-parameters are captured with a Vector Network Analyzer (VNA, Agilent E8361A).

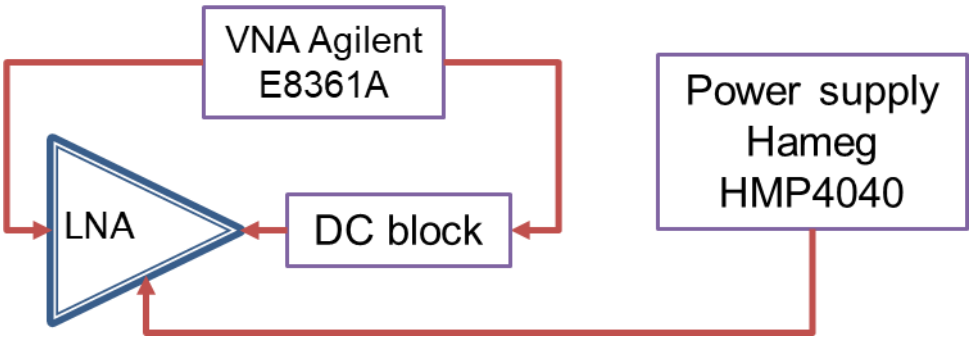
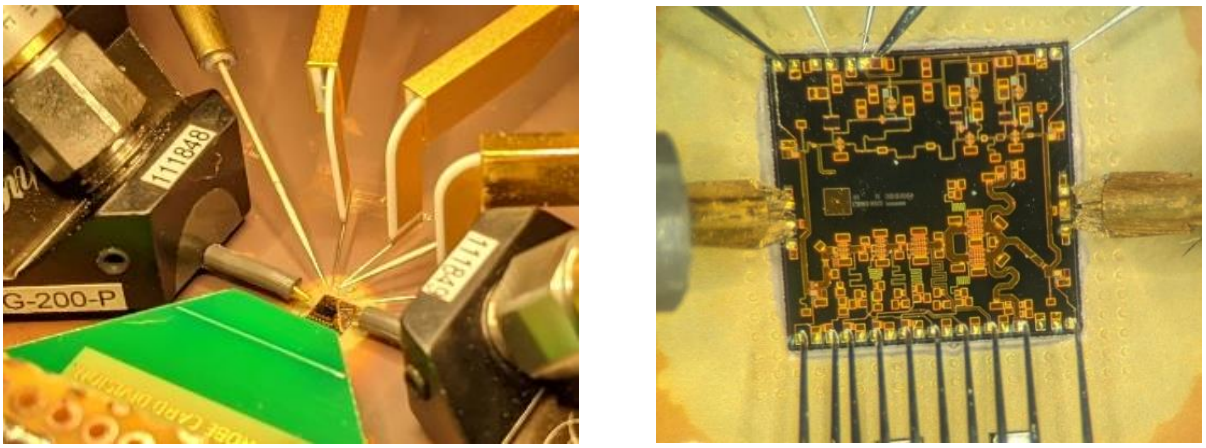


Figure 30 Block diagram of the LNA measurement test setup

To validate the embedding process for the amplifier IC each critical step was validated. The RF performance of the airbridges is sensitive to changes in the geometry and surrounding material properties. Therefore the impact of the assembly and the initial embedding were tested. The test is based on a comparison of the RF performance of the LNA part of the IC before and after processing.

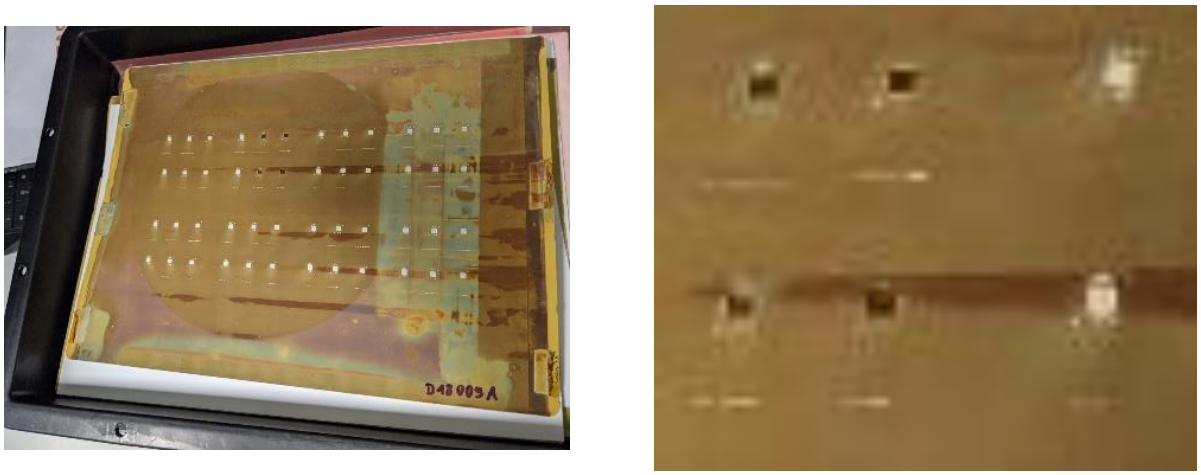
Figure 31 shows the details of probing of an OMMIC GaN power amplifier IC with the RF GSG probes and the DC needles. The biasing of the LNA and the switches, which changes the RF path between Rx and Tx mode, follows the input provided by OMMIC.



(a) (b)

Figure 31 Test setup of LNA measurement. (a) Overview of probed IC. (b) Enlarged view on probed IC.

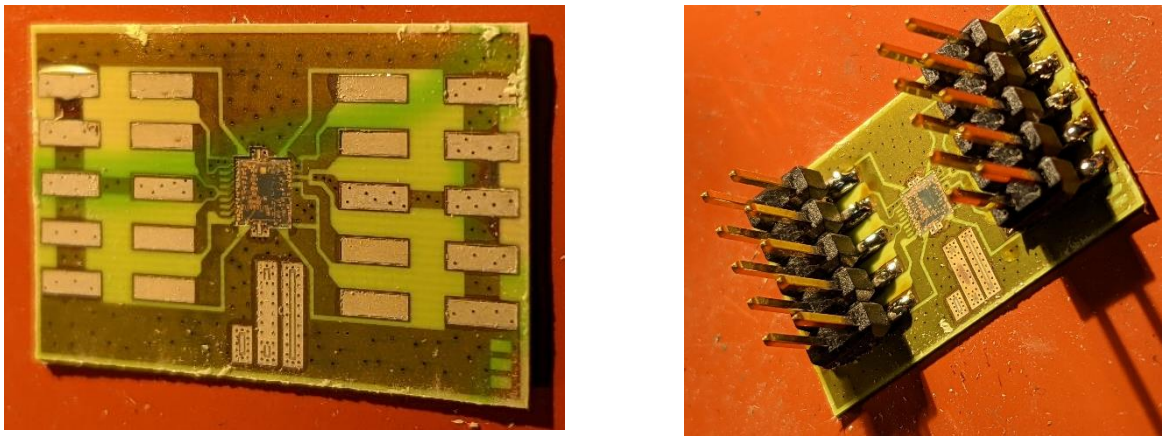
Next, another measurment using the same setup as the bare-die measurement above was performed after assembly and glueing of the dies onto the PCB substrate. The manufactured panel containing the assembled ICs can be seen in Figure 32. Here, the pressure needed for the pick-and-place and the sinter glueing was optimized to prevent damaging the ICs.



(a) (b)

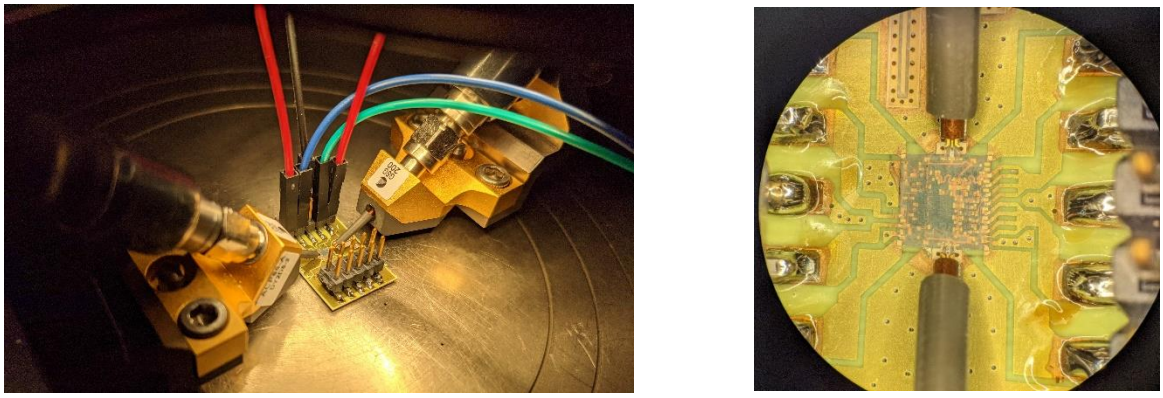
Figure 32 Board with four assembled ICs. (a) Complete board (b) detailed view of ICs assembled to board

After the assembly of the chips, the build-up film is processed onto the panel having the first copper layer for signal distribution on top. On this layer, the fan-out of the chip is realized. Therefore, all supplies are routed to pads for pin headers, and the RF landing pads are designed to match a characteristic impedance of 50Ω. This approach allows to remove the DC needle for the supplies in the aforementioned measurement setup while the RF pads are still contacted with GSG probes. This setup is illustrated in Figure 33 and Figure 34.



(a) (b)

Figure 33 Manufactured test package for the PA/LNA IC. (a) Embedded IC in PCB. (b) Test package including pin headers for supplies



(a) (b)

Figure 34 Measurement setup of the embedded ICs. (a) Overview of the setup. (b) Enlarged view of the probing sections.

4.1.2 Measurement results

Bare die measurements of the LNA part of the GaN ICs were performed to receive initial performance characteristics. The result of the S21 measurement can be seen in Figure 35. The gain is 14 dB within the frequency band of interest, i.e. 37-40 GHz, showing similar performance to the measurements at OMMIC [6].

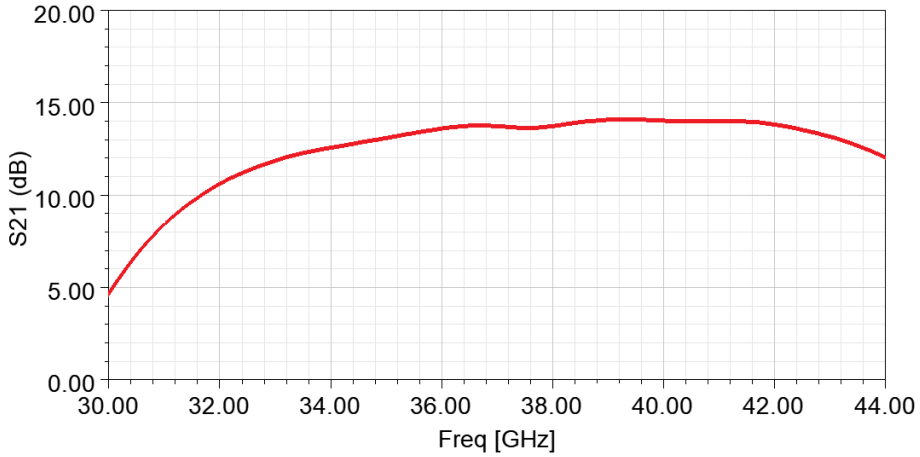


Figure 35 Gain of the LNA carried out in the bare-die measurement.

After the pick-and-place process, the measurement of the LNA performance shows a good correlation between pre- and post-assembly, with variations < 1 dB (cf. Figure 36), four assembled ICs results from the same board from Figure 32 (b).

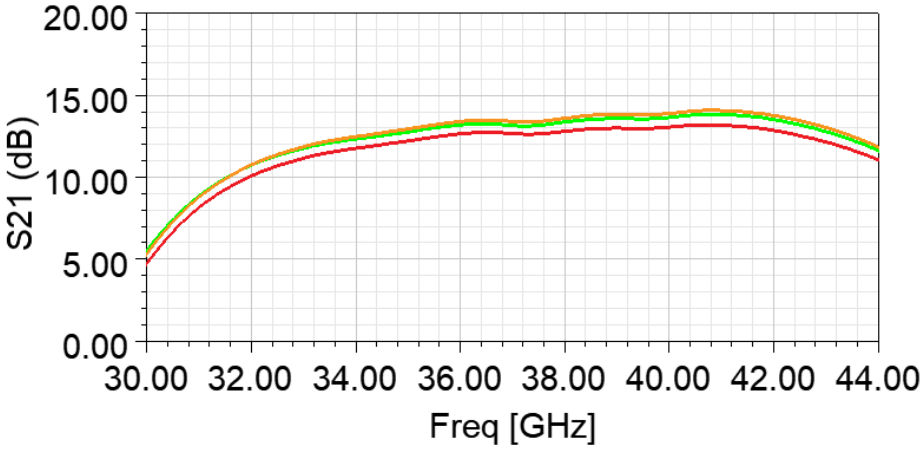


Figure 36 Measurement results of assembled ICs

	IC1	IC2	IC3	IC4
Gain S21[dB]	14	13	13	14

Table 1 Gain of the measured ICs at 39 GHz

In Figure 37, the S_{21} curve for an embedded IC is shown. Again, the gain reaches up to 14 dB between 37-40 GHz, and compared to the results of the previous manufacturing steps, the curves are similar.

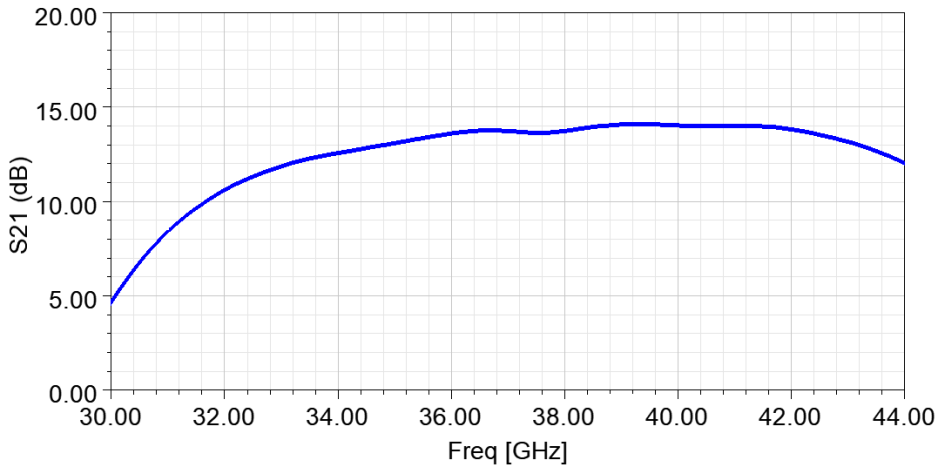


Figure 37 LNA measurement of embedded OMMIC ICs LNA measurement of embedded OMMIC ICs

In summary, the critical manufacturing steps could be optimized and were verified by several measurements at different processing stages.

4.2 Low-Power Modules

4.2.1 Measurement Set-Up

In order to validate the functionality of the embedded low-power modules, a basic functionality test of the fabricated modules was performed. Two different test boards were designed in collaboration with the partner TUB. These boards serve as interface between the packaged ICs and the measurement equipment (Figure 38).

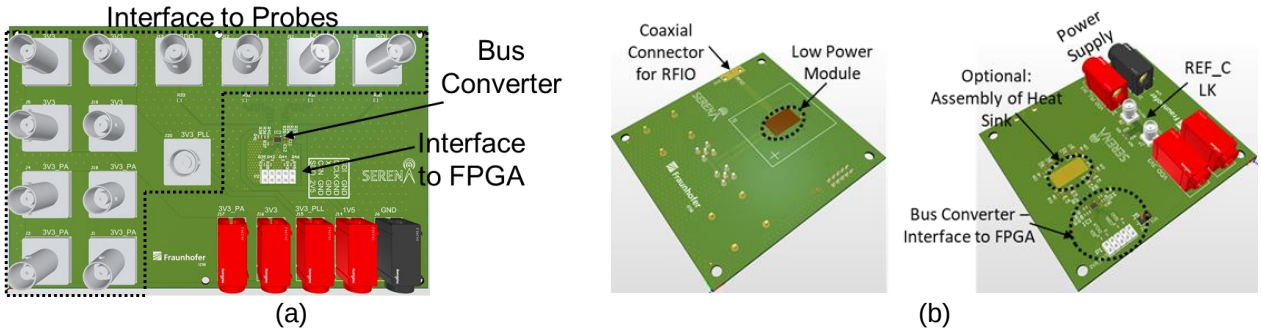


Figure 38 Test boards for low-power module (a) Interface board (b) RF test board

Figure 39 shows the first assembled embedded low power module on the PCB test board.

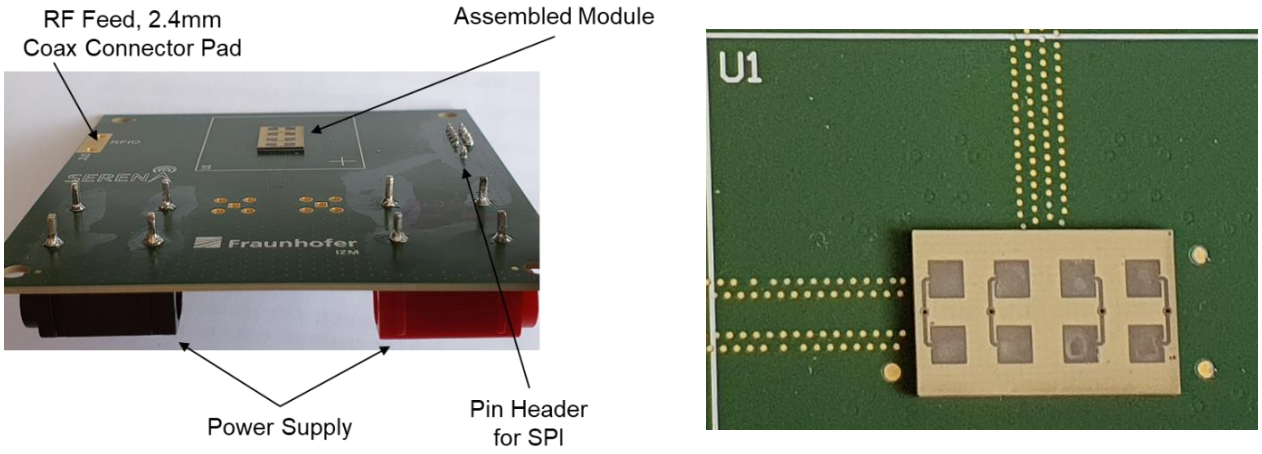


Figure 39 First assembled low-power module on the test board

The basic alive test is a non-destructive test of the low power modules. The target is to verify the functionality of the IC's digital communication interface, i.e. the serial peripheral interface (SPI). A test routine was provided by TUB, which runs fundamental commands the chip is able to execute. This commands are as follows:

1. Checking the status of the IC: This test returns that the chip is powered and selected for further processing.
2. Testing registers' read/write: Here, the registers' default value is checked, then a new value is written, and will be read back.
3. Testing BITE power (ADC): This test increases the current drawn at the VDD pin by ~ 10 mA.
4. Testing of RF power: The current drawn at the VDD pin is increased by ~ 100 mA.
5. MBIST tests of the IC: This test should print "MBIST test successful".

There is also a sixth test available, which execute a temperatue measurement. However, this requires an external differentially fed reference clock signal, which will not be applied in this setup due to the limited availability of suitable probing needles. In order to power the IC and run the different routines, the modules were placed on a wafer prober system with the module's LGA interface facing upwards. Furthermore, the minimum requirements for powering up the IC is chosen, and the respective LGA pads are connected through DC needles. In addition to the supplies and reference, the four pads for the SPI have to be probed using the same DC needles. In total, seven positions need to be probed in this minimal setup. A module is classified as functional, as soon as the first test returns "PON" (power on), and the third test causes the increase of current draw on the VDD rail by 10 mA. However, the other tests are not taken into account, since a full supply would be necessary here.

The interface board in Figure 39 is required as a physical interface between measurement equipment, e.g. power supplies, and the packaged modules. In addition, the interface board provides a translation for the SPI signals between the Beamer IC, and the used FPGA by applying a bus converter by Texas Instruments (SN74AXC4T774RSVR). This is necessary in order to match the Beamer IC's SPI signal levels at 1.5V to the required 3.3V of the FPGA.

This test routine is performed with each low power module to categorize them as passed or failed modules., the passed ones are delivered to Ericsson for the assembly onto their system board for the final demonstration.

On the other hand, a second PCB is designed for advanced testing of the low power modules. This RF test board, see top and bottom side of this PCB in Figure 38 (b), contains the same functionalities like the interface board, i.e. providing supplies, and voltage translation. Additionally, the RF test

board accomodates the landing pads for the LGA interface of the low power module for direct assembly, and a coaxial connector for the 39 GHz signals, which convey the high frequency signals to/from the package. Therefore, this setup provides the optimal power supply of the modules, since all pins can be connected. In addition, RF testing of the low power modules can be performed, i.e. radiation or reception of 39 GHz signals via the package integrated antennas. However, this assembly of modules cannot be reversed, and will just be performed with a few components for initial RF tests.

4.2.2 Measurement results

An initial measurement of bare die beamformer ICs has been carried out using the non-destructive setup in order to have a reference for the packaged module, see Figure 40.

```
test 1/6
checking BEAM39PA status
this should print "status (0x4080): PON LOCK" after power on and "status (0x0000):" after reruning this test
**
M1B1: status (0x4100): PON
**
clearing and checking BEAM39PA status, this should print "status (0x0000):"
cleared status registers
**
M1B1: status (0x0000):
**
reseting all BEAM39PAs to be in a known state: resetting SERENA system
press enter to continue, ctrl+c to stop

test 2/6
testing register read/write of the BEAM39PA
This test uses the register PLL_CTRL_1. It tests for the default value, writes a value and reads it back.
testing BEAM39PA M1B1
  reading default value:
  * reading successful, default value wrong
  writing test value
  reading test value:
  * reading successful, value wrong
  writing back default value
press enter to continue, ctrl+c to stop

test 3/6
testing BITE power (ADC), this should increase the current drawn at the VDD pin by probably >10mA
testing BEAM39PA M1B1
  press enter to enable the ADC
  * ADC enabled
  press enter disable the ADC
press enter to continue, ctrl+c to stop

test 4/6
testing RF power, VDDPA supply required.
Are the VDDPA pins and all VDD pins connected? Press "y" and enter for yes, just enter for no:
skipping RF power test.
press enter to continue, ctrl+c to stop

test 5/6
running MBIST tests of the BEAM39PAs, this should print "MBIST test successful"
  * Error using MmdSerenaBeamer/run_mbist (line 2532)
M1B1: error reading MBIST result or not done, code 0, mbist reg FF20
```

(a)

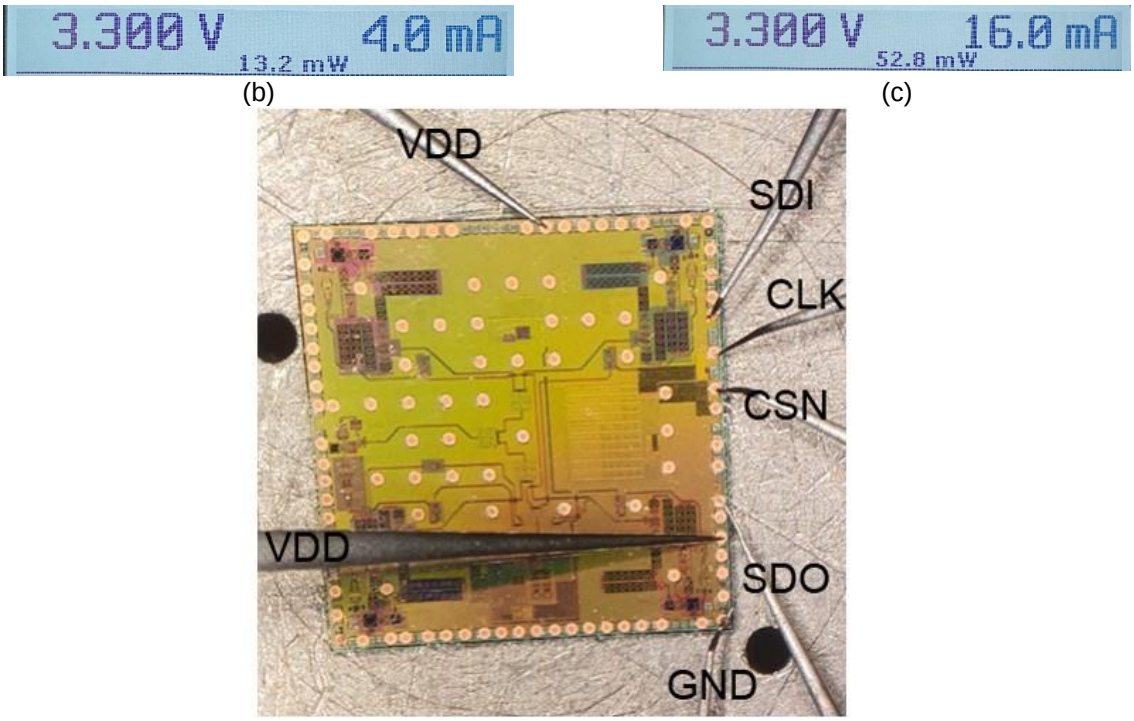


Figure 40 Bare die result of test routine for SPI communication in non-destructive setup

Due to the limited number of voltage supply DC needles, not all the tests fully passed. However, the criteria for a passed module could be defined from test 1, which returns the power on state, and from test 3, where an increase in current consumption could be detected on the Vdd rail, as can be seen in Figure 40(b) and (c), which shows a communication could be established. Next, the bare dies were replaced by the packaged samples using the same connection with DC needles as before, see Figure 41.

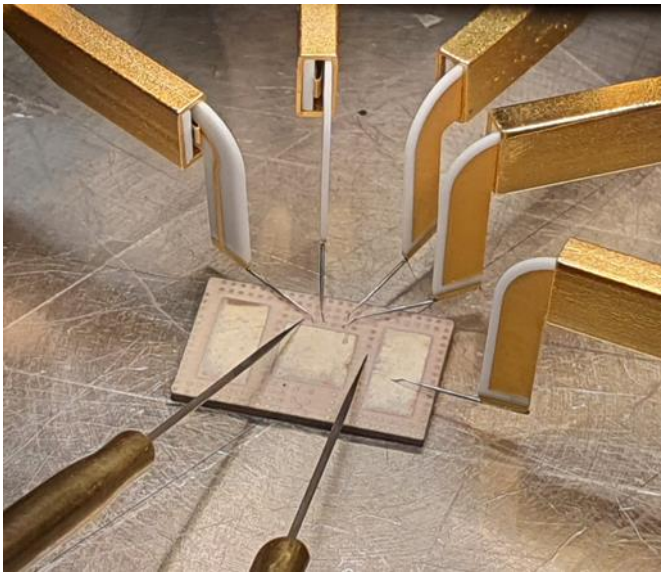


Figure 41 Measurement setup for packaged modules

This test procedure was executed on all available low power modules. Nine passed samples were delivered to the partner Ericsson for the assembly onto their systemboards.

A remaining low power module was assembled onto the second test board, see Figure 39. In Figure 42, the measurement environment is shown for the RF test board including the assembled low power modules.

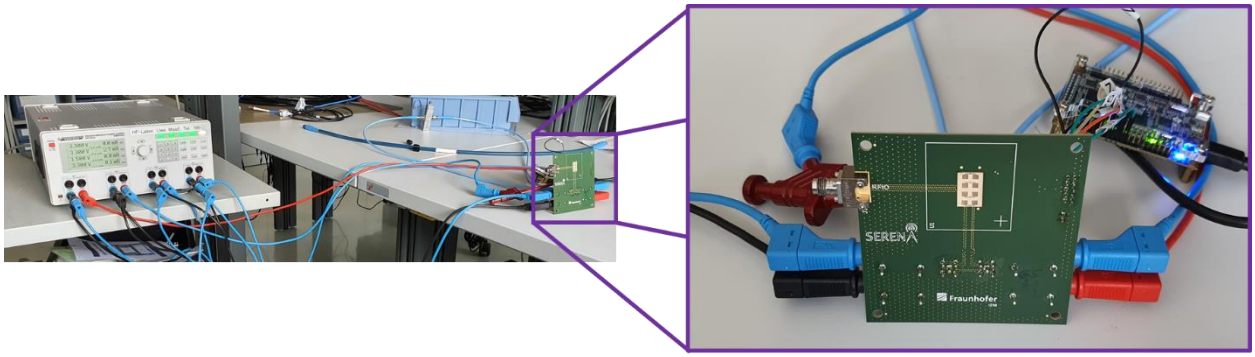


Figure 42 Measurement setup for packaged modules assembled on test board

The purpose of this setup is the verification that a low power module, which passed the basic alive test in the probe measurements, passes also the complete test routine. Therefore, the RF test board provides the packaged sample with all the required supplies, SPI, and RF connections. The test results from the measurement setup in Figure 42 are as shown in Figure 43. The packaged module assembled on the test board passes all the tests and behaves as expected.

```
test 1/6
checking BEAM39PA status
this should print "status (0x4080): PON LOCK" after power on and "status (0x0000):" after reruning this test
**
M1B1: status (0x4080): PON LOCK
**
clearing and checking BEAM39PA status, this should print "status (0x0000):“
cleared status registers
**
M1B1: status (0x0000):
**
reseting all BEAM39PAs to be in a known state: resetting SERENA system
press enter to continue, ctrl+c to stoptest

2/6
testing register read/write of the BEAM39PA
This test uses the register PLL_CTRL_1. It tests for the default value, writes a value and reads it back.
testing BEAM39PA M1B1
  reading default value:
  * reading successful, default value correct
  writing test value
  reading test value:
  * reading successful, value correct
  writing back default value
press enter to continue, ctrl+c to stop test

3/6
testing BITE power (ADC), this should increase the current drawn at the VDD pin by probably >10mA
testing BEAM39PA M1B1
  press enter to enable the ADC
  * ADC enabled
  press enter disable the ADC
press enter to continue, ctrl+c to stoptest

4/6
testing RF power, VDDPA supply required.
Are the VDDPA pins and all VDD pins connected? Press "y" and enter for yes, just enter for no:
 ypowering up the common channel and channel 0 in RX mode, current drawing should increase by roughly 120mA.
testing BEAM39PA M1B1
  press enter to power common channel and channel 0 up
  * M1B1: powered up  press enter to power common channel and channel 0 down again
  * M1B1: powered down
press enter to continue, ctrl+c to stoptest

5/6
running MBIST tests of the BEAM39PAs, this should print "MBIST test successful“
  * M1B1: MBIST test successful
press enter to continue, ctrl+c to stoptest
```

(a)

(b)

(c)

(d)

Figure 43 Outcome of tested assembled low power module

Chapter 5 Summary and Conclusion

In conclusion, high power and low power modules were designed. Fabrication of lower power modules was successful. The approach for having an initial test for basic functionalities on low power modules, which is non-destructive, has been successful. It could be shown, that the digital block of the Beamer IC is functioning after the chip embedding and the processing of the different PCB layers. Although only two out of five tests could be performed from this minimal setup, these are conclusive enough to assign the modules as functional. In the RF test board setup, the low power modules will pass the complete test routine due to the full availability of the needed supplies. Functionality of embedding of OMMIC PA were done with multistep measurement and embedding, thus enabling the packaging of OMMIC PA with airbridges inside the IC.

Major Technical Achievements:

- Successful design and fabrication of low-power embedding module.
- Successful design and fabrication of test board for low-power modules
- Successful testing of fabricated modules using DC probes and designed test board
- Successful embedding of OMMIC amplifier ICs with air bridges and thin gold pads for contacting OMMIC amplifier ICs

Chapter 6 List of Abbreviations

Abbreviation	Translation
PCB	Printed circuit board
mmwave	Millimeter wave
5G	Fifth generation
AiP	Antenna-in-package
LGA	Land grid array
PA	Power amplifier
ABF	Ajinomoto build-up film
IC	Integrated circuits
RF	Radio frequency
GHz	Gigahertz

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[6] SERENA project: Dies delivery RUN1 39GHz Demo Chips, Deliverable D2.3